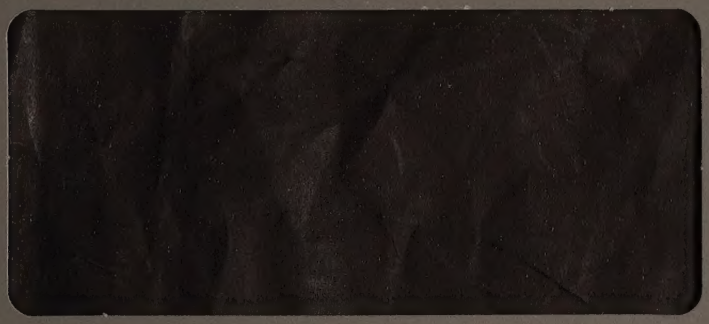
Operator's Manual



LeCroy

Innovators in Instrumentation

MODEL 6810
WAVEFORM RECORDER

Preliminary Information

September, 1987

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration,

and use of LeCroy equipment are available from the Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499 (914) 578-6059, or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support service. For example, Blue Ribbon service provides guaranteed three-day turn around on repairs, a direct access number for product application assistance, yearly calibration and the addition of engineering improvements. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.

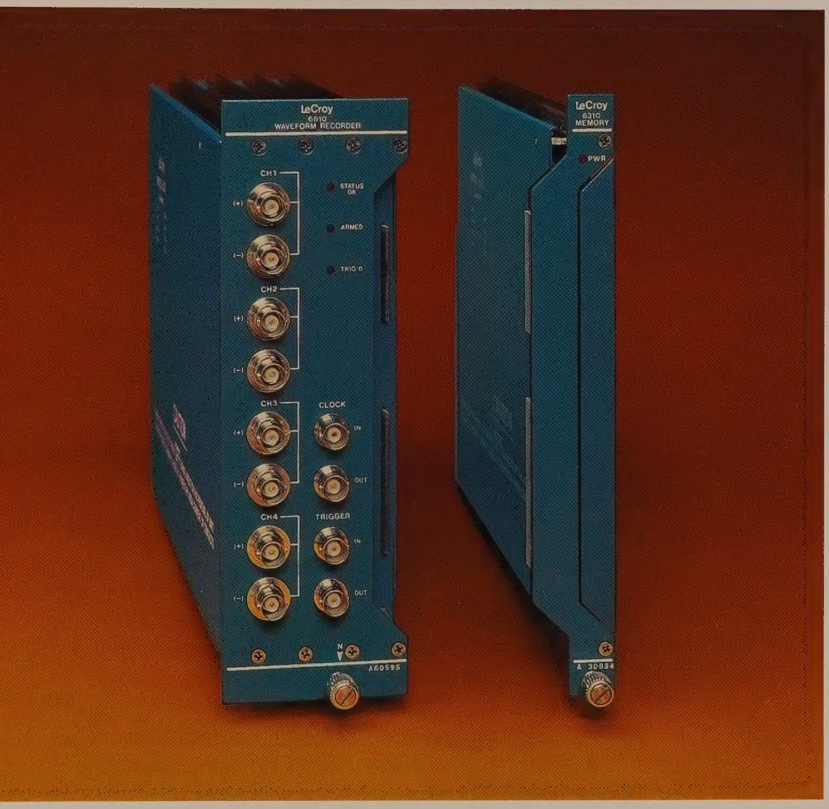
- Modify the software and/or merge it into another program for your use on a single machine.

- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

WAVEFORM DIGITIZER
4 CHANNEL, HIGH RESOLUTION

LeCroy

6810 WAVEFORM RECORDER
6310 MEMORY



- 1, 2 or 4 channel simultaneous waveform sampling
- 5 megasample/second max. digitizing rate
- 12 bit vertical resolution
- Up to 8 million samples of memory
- Up to 100 Volt differential inputs
- Over 4000 waveforms/second capture rate
- Trigger-point arrival time buffers
- Window and hysteresis triggering modes

HIGH RESOLUTION RECORDING OF LONG SINGLE-SHOT WAVEFORMS

The LeCroy 6810 Waveform Digitizing/Recording system captures entire single-shot waveforms using digital storage techniques. Conversion of your analog waveform into digital data simplifies waveform analysis and allows storage on floppy disks and hardcopies on printers.

The LeCroy 6810 combines powerful waveform recording features not found on instruments costing many times more. These 6810 features mean simple solutions for applications including:

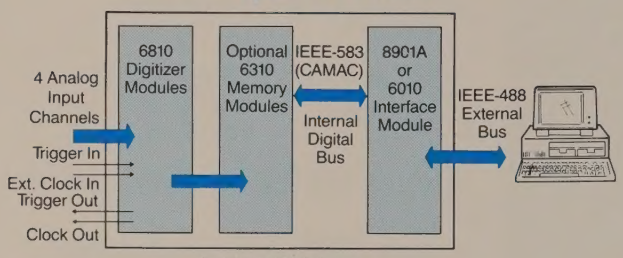
- power monitoring
- high voltage testing
- noise and vibration testing
- automotive testing
- geology/seismology monitoring
- ballistics/explosives testing
- materials studies
- biomedical research
- power supply testing and other ATE
- sonar, radar and ultrasonics
- magnetic media testing

PRODUCT DESCRIPTION

MEETS YOUR NEEDS TODAY AND TOMORROW

The LeCroy Model 6810 Waveform Recorder module is a complete independent recording system. Thus it provides unprecedented total system performance for measuring DC to 2.5 MHz signals. The 6810 includes wide range differential amplifiers, track and holds, a high resolution analog to digital converter (ADC), powerful triggering circuitry and on-board waveform memory. The memory can be expanded via Model 6310 Memory modules.

System Architecture

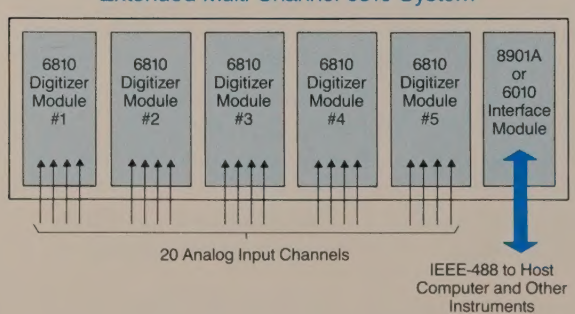


The 6810 conforms to the IEEE-583 Standard (CAMAC) for form factor, power consumption, and programming codes format. This modularity prevents system obsolescence and ensures simple expandability. The 6810 digitizer is totally compatible with the full line of LeCroy modular digitizers and other instrumentation. You can add other digitizers to your system to cover an even wider range of sample rates.

TURNKEY CONFIGURATIONS

The Model 6810 Waveform Recorder can be purchased in a turnkey 4-channel Century Series™ 2005 (benchtop mainframe) or 2005RM (rack-mount mainframe) starter system. Or the 6810 module itself can be added into an existing Century Series system for expansion:

Extended Multi-Channel 6810 System


6810 Digitizer Module #1
6810 Digitizer Module #2
6810 Digitizer Module #3
6810 Digitizer Module #4
6810 Digitizer Module #5
8901A or 6010 Interface Module
20 Analog Input Channels
IEEE-488 to Host Computer and Other Instruments

The benchtop mainframe can hold two 6810 modules for up to 8 channels. The rackmount mainframe can hold five 6810 modules for up to 20 channels. One IEEE-488 Standard interface port allows up to 280 channels in one system via 14 mainframes.

The Century Series includes one 6810 module, an instrument mainframe, an IEEE-488 Standard (GPIB) interface, a GPIB cable, and PC-based WAVEFORM-CATALYST™ Oscilloscope software. WAVEFORM-CATALYST integrates an IBM-PC/XT/AT/Personal System 2™ or COMPAQ III/386™ and the Century Series into a multi-channel waveform recording system. It simplifies waveform capture, display, analysis and disk storage.

The 6810 also operates with ASYST™ software for Fast Fourier Transforms (FFT) and multichannel waveform math.

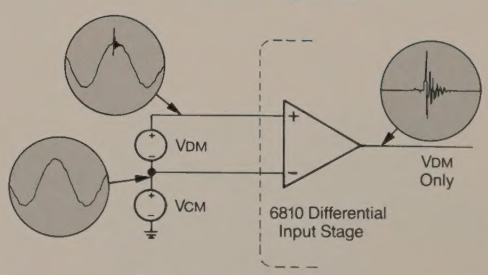
DIFFERENTIAL INPUT CHANNELS

The 6810 Digitizer module contains four input channels with independent configuration, gain, offset and AC or DC coupling. Each channel has both a non-inverting (+) and an inverting (–) input connector. The connectors can be configured in four different combinations:

- DIFFERENTIAL (both + and – active)
- NON-INVERTING (+ active, – grounded)
- INVERTING (+ grounded, – active)
- GROUNDED (both + and – grounded)

Single-ended inputs can allow external electrical noise to mix with the desired waveform. But the 6810 differential inputs reject common mode noise and transducer bias voltages. They measure only the voltage difference between the inputs.

Common Mode Voltage Rejection

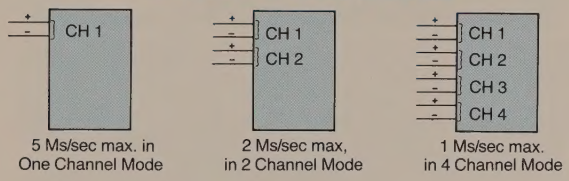


The 6810 module uses one selectable setting for all four channels for memory length, sample rate, pre-trigger waveform length, trigger delay time and trigger source.

FLEXIBLE TIMEBASE SETUPS

The 6810 sample rate can be programmed from 20 samples per second up to 5 million samples per second. The sample rate steps occur in a 1, 2, 5 sequence, just like an oscilloscope. The maximum sample rate depends upon the number of active channels:

Maximum Sample Rates
vs. Number of Active Channels



5 Ms/sec max. in One Channel Mode

2 Ms/sec max, in 2 Channel Mode

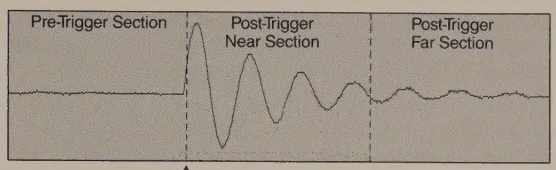
1 Ms/sec max. in 4 Channel Mode

The 6810 can also use an external clock source to establish the sample rate. Thus the 6810 can be synchronized to your experiment or test. The external source can be any frequency from DC up to 5 MHz.

SPECIAL DUAL TIMEBASE

A special dual timebase mode conserves waveform memory. It changes the sample rate during a waveform acquisition. A fast sample rate resolves detailed waveform sections. A slower rate conserves memory at other times. The user may select any two sample rates.

The user may assign either sample rate, f1 or f2, to the pre-trigger waveform section, the post-trigger-near section and the post-trigger-far section. When in segmented memory mode, (see "Memory Segmentation") these three sections apply to each individual memory segment. Three f1/f2 combinations exist:



1)	f_1	f_2	f_1
2)	f_1	f_2	f_2
3)	f_1	f_1	f_2

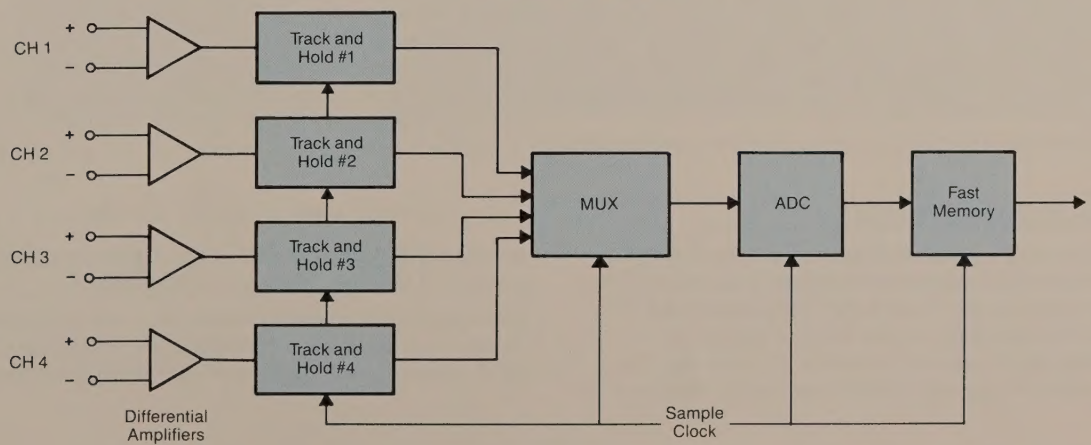
The user also selects the post-trigger-near section size. It may be as small as 4 samples or as large as all the post-trigger samples.

SIMULTANEOUS MEASUREMENTS

Accurate multichannel comparisons and analysis, such as current and voltage monitoring for power calculations, demand simultaneous sampling. The 6810 uses track and hold circuits on each input channel (see 6810 Block Diagram). One sample clock controls all track and holds. Therefore, all four channels sample their inputs simultaneously, rather than sequentially like most other multiplexed systems.

Also, the LeCroy 6810 superb channel isolation prevents voltages on one channel from corrupting measurements on another channel.

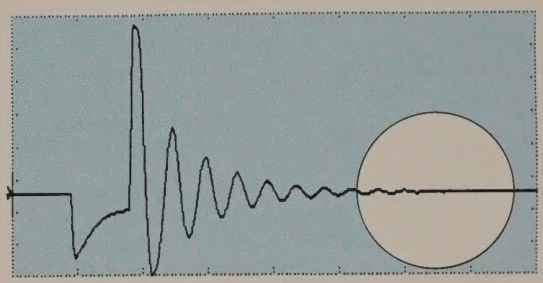
6810 Block Diagram



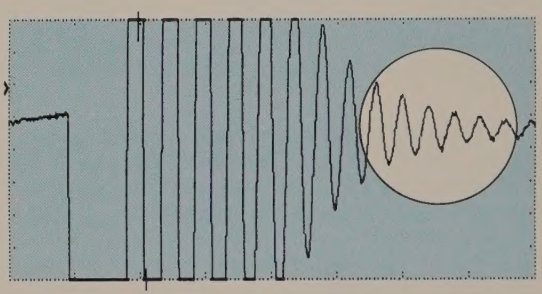
HIGH VERTICAL RESOLUTION

The 6810 contains a high accuracy, 12-bit resolution, analog to digital converter. In addition, each 6810 channel has eight input ranges from 400 mV to 100 V full scale. The combination of high resolution and multiple ranges means the 6810 can accurately record a waveform of almost any amplitude.

12-bit resolution equates to 4096 different detectable input levels. Thus, the 6810 can measure 100 μV changes when on the 400 mV range. Repetitive-waveform averaging in the host computer further increases this resolution.



No Vertical Expansion



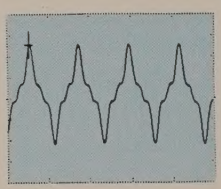
X16 Vertical Expansion

The 12-bit resolution 6810 captures much more detail than can be displayed on a computer display screen. Therefore, LeCroy's WAVEFORM-CATALYST software features vertical expansion. This zoom capability exposes details not at first visible on the screen. The screen cursors always present the full resolution via digital readouts.

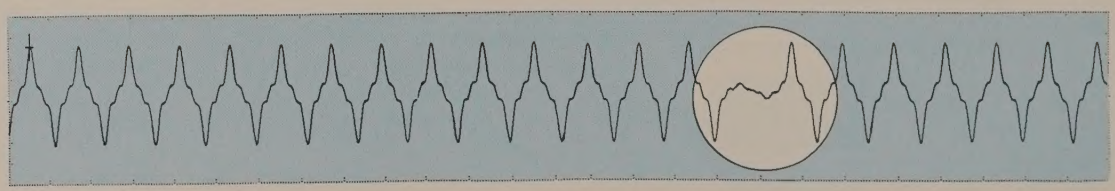
DEEP WAVEFORM MEMORY

The 6810 stores digitized waveform data in fast memory. The 6810 module contains 512k samples of memory. Model 6310 Memory Expansion modules add 512k samples each. A maximum of 15 memory modules expand the system memory to 8 megasamples.

The 8 megasample system supplies a full 8 seconds of continuous recording time at 1 megasample/sec sample rate or more than 6 minutes at 20 ksamples/sec.



512k Samples Standard



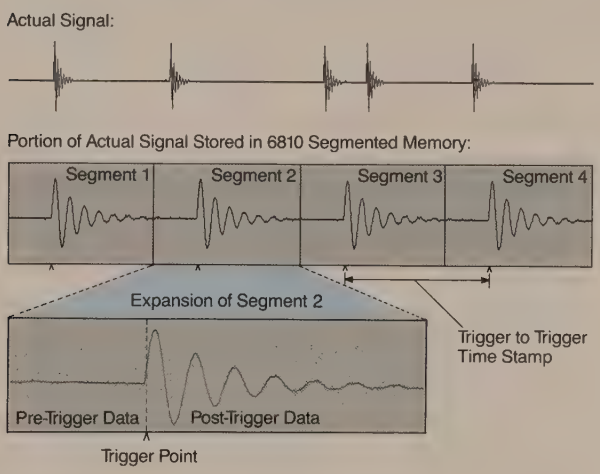
Expandable to 8M Samples Using Model 6310 Memory Modules

MEMORY SEGMENTATION

The 6810 memory can be divided into a maximum of 1024 segments. Each segment requires a separate trigger signal to initiate recording. Thus, numerous pulses can be recorded quickly without emptying memory after each capture and without recording the deadtime between pulses. In this segmented memory mode, the 6810 can record up to 4880 waveforms per second (5 MS/sec, 1024 point segment).

The segmented memory mode also helps to precisely reconstruct the timing of intermittent waveforms. The 6810 records the trigger-to-trigger times from segment

to segment. This trigger time stamp clock has variable resolution. And the long time stamp buffer shows up to 72 minutes between triggers with 1 μsec resolution, up to 16 months with 10 msec resolution.



POWERFUL TRIGGER MODES

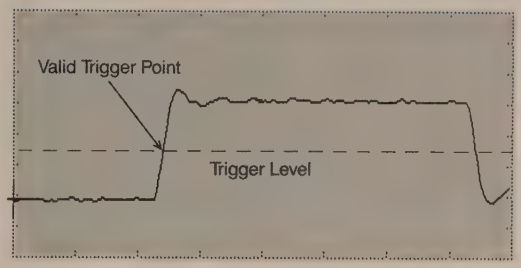
All active 6810 input channels use the same trigger. The 6810 module will trigger when the trigger source meets specific waveform conditions or when a software trigger command occurs. Either an external trigger input, the channel 1 signal or the channel 2 signal can act as the trigger source.

After the 6810 has been "Armed", the digitizer begins filling memory. At the end of the memory segment it returns to the beginning and overwrites continually until it receives a trigger. If the entire waveform memory segment is configured for pre-trigger data, then the 6810 stops filling the memory segment when the trigger condition is met. If the entire waveform memory segment is configured for post-trigger data (0% pre-trigger), then the 6810 fills the memory "circle" one more time after a valid trigger. The percentage of pre-trigger data can be selected in 1/8ths of the total memory size.

The 6810 supplies five different trigger condition selections:

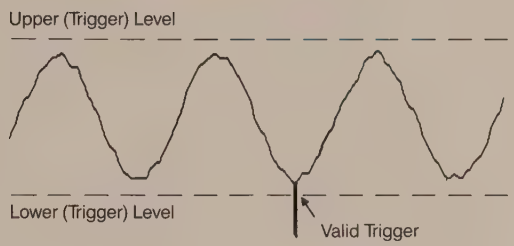
- POSITIVE SLOPE
- NEGATIVE SLOPE
- WINDOW
- POSITIVE HYSTERESIS
- NEGATIVE HYSTERESIS

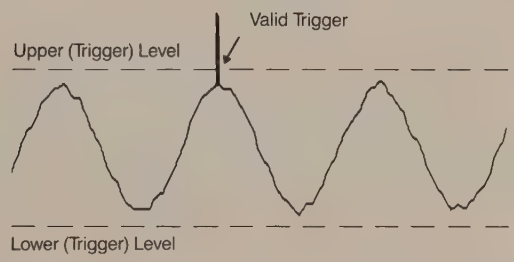
Positive Slope Triggering



Positive or Negative Slope triggering simply occurs at a selected voltage level on the positive or negative slope of the trigger source signal.

Window Triggering

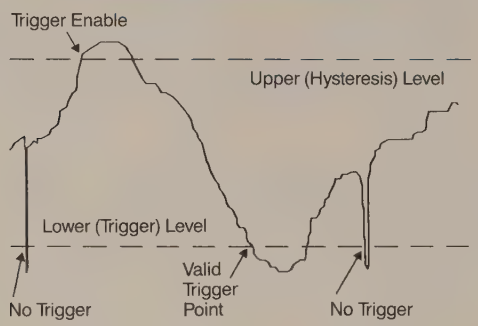




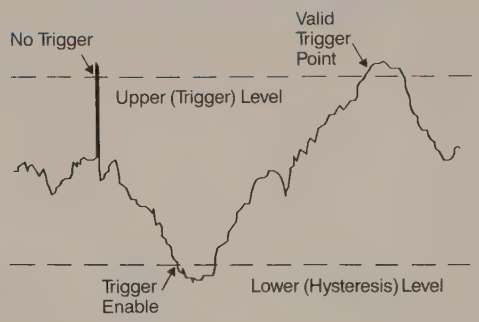
Window triggering occurs when the trigger source signal passes in a positive direction through an upper trigger level or in a negative direction through a lower trigger level. The upper and lower levels are independent user-selected voltages.

Positive and Negative Hysteresis triggering makes the trigger point less susceptible to noise. A trigger will only occur after the signal has crossed a hysteresis level. This level can be thought of as a "trigger enable."

Positive Hysteresis Triggering



Negative Hysteresis Triggering



FULL REMOTE CONTROL

All 6810 functions (gain, offset, coupling, etc.) are programmable and can be controlled remotely via the IEEE-488 Standard interface bus (GPIB). Either Model 8901A or Model 6010 interface modules provide this bidirectional GPIB communication. A host computer can download control and setup commands to the 6810 and upload waveforms from the 6810. The 8901A interface uploads at up to 225 ksamples per second; the 6010 at up to 100k samples per second.

SPECIFICATIONS

All specifications refer to the guaranteed minimum performance of the entire 6810/6310 digitizing system. All selectable parameters are IEEE-488 bus and IEEE-583 (CAMAC) bus programmable.

TOTAL DYNAMIC ACCURACY

Signal Frequency	Signal-to-Noise Ratio	Harmonic Distortion
200 kHz	67 dB	– 70 dB
1.0 MHz	66 dB	– 68 dB
2.5 MHz	62 dB	– 62 dB

Performance measured by comparing a digitized bipolar 95% FS sinewave using internal 5 MHz clock against ideal results.

ANALOG INPUTS

Connectors: 2 BNC type coaxial per channel (+ and –)

Quantity: 4 input channels, simultaneously sampled

Active Number of Channels: 1, 2 or 4

Channel Isolation: 66 dB minimum between any two channels

Input Modes:
1. Differential (both + and – active)
2. Non-inverting (+ active, – grounded)
3. Inverting (– active, + grounded)
4. Both connectors grounded

Common Mode Rejection Ratio (differential input mode):
0.4V, 1V, 2V, 4V ranges:
66 dB @ DC, 50/60 Hz, 400 Hz
63 dB @ 100 kHz
10V, 25V, 50V, 100V ranges:
54 dB @ DC, 50/60 Hz, 400 Hz
51 dB @ 50 kHz

Common Mode Voltage: 125V max. on 10V, 25V, 50V and 100V ranges
5V max. on 0.4V, 1V, 2V, and 4V ranges

Bandwidth: DC to 2.5 MHz minimum

Pulse Response: Tr <120 nsec, with <5% overshoot

Coupling: AC or DC

Input Impedance: 1 MOhm, 40 pF

Voltage Range: Selectable in 8 steps

Full scale Input voltage	Sensitivity
400 mV	100 μV
1 V	250 μV
2 V	500 μV
4 V	1 mV
10 V	2.5 mV
25 V	6.25 mV
50 V	12.5 mV
100 V	25 mV

Overload Protection: ±100 V AC or DC continuous

Overload Recovery Time: 1 μsec to within ±1.5% from a 3X full scale, 10 μsec duration input

DC Gain Non-linearity: ±0.1% maximum of full scale

Offset: Up to ±50% full scale. Selectable in 256 steps

TIMEBASE

Internal Sample Clock Rates:

5M samples/sec*	10k samples/sec
2M samples/sec**	5k samples/sec
1M samples/sec	2k samples/sec
500k samples/sec	1k samples/sec
200k samples/sec	500 samples/sec
100k samples/sec	200 samples/sec
50k samples/sec	100 samples/sec
20k samples/sec	50 samples/sec
	20 samples/sec

*1 channel mode only
**1 or 2 channel modes only

Dual Timebase: 2 selectable timebase changes within each memory segment.
Sample rate changes at trigger point and 'N' samples after the trigger point in any combination:

PRE-TRIGGER	POST-TRIGGER NEAR	POST-TRIGGER FAR
rate 1	rate 1	rate 1
rate 1	rate 2	rate 1
rate 1	rate 2	rate 2
rate 1	rate 1	rate 2

Sample rate 1 and rate 2 may be any of the internal rates
Clock In disabled in dual timebase mode, Clock Out available

Clock In: BNC connector
Any external frequency from DC to 5 MHz
Must be a 74 HC series TTL compatible signal

Clock Out: BNC connector
Buffered internal sample clock
50 Ohms drive capability
Short circuit protected
40 nsec maximum propagation delay "Clock In" to "Clock Out"

ANALOG TO DIGITAL CONVERSION

Resolution: 1 : 4096 (12 bits)

Aperture Uncertainty: <50 psec @ 5 MHz internal clock rate

TRIGGERING

Minimum Trigger Signal Duration: 50 nsec

Trigger Source: Selectable from either external (Trigger In), internal or manual (bus command)

Trigger In: BNC connector
1 MOhm input impedance
Protected to ±50V
Range from −5V to +5V

Internal Trigger: Pickoff from channel 1 or 2
Range from − Full scale to + Full scale

Trigger Level: 256 steps across range
1 level for single slope trigger modes
2 independent levels for window and hysteresis modes

Trigger Modes: Positive slope
Negative slope
Window
Positive hysteresis
Negative hysteresis

Trigger Coupling: DC
AC
Low frequency reject (−3 dB @ 36kHz, 20 dB/decade roll off)
High frequency reject (−3 dB @ 36 kHz, 20 dB/decade roll off)

Trigger Not Accepted During:
1. Programmed "Trigger Disable"
2. Pre-trigger recording when "Trigger Holdoff" enabled
3. Post-trigger recording
4. First 160 μsec after last post-trigger sample in the previous memory segment

Trigger Out: BNC connector
Trigger signal for synchronized multiple 6810 operation
50 Ohms drive capability
Short circuit protected
80 nsec maximum propagation delay "Trigger In" or internal trigger to "Trigger Out"

Pre-trigger: Portion of memory filled with waveform data occurring before valid trigger condition.
Selectable in 1/8ths of the memory segment length from 0/8 (100% post trigger, no-trigger data) to −8/8 (100% pre-trigger data).

Delayed Trigger: Time delay from valid trigger condition to the start of memory segment recording.
Selectable time T = (L)(S)(P) where:
L = selectable memory segment length fractions (1/8 to 247/8)
S = number of samples per memory segment
P = sample interval

Example: Sampling at 1MS/sec with a segment length of 4096 samples and a delay trigger setting of 19/8 yields 9.73 msec delay after the trigger before recording begins.
(1 μsec/sample)(4096)(19/8) = 9.73 msec

Time Stamps: The elapsed time from Arm to first Trigger, from first Trigger to second Trigger, and so on, each value stored in a buffer
Applies when number of channel memory segments >1

1024 time stamp buffers (bus readable as a block)
32-bit resolution
Selectable time sensitivity:

Sensitivity (1 bit)	Maximum Representable Time Before Buffer Rollover (32 bits)
1 μsec	71.58 minutes
10 μsec	11.93 hours
100 μsec	4.97 days
1 msec	49.71 days
10 msec	>16 months

WAVEFORM MEMORY

Internal: 512k samples

Expansion: Additional 512k samples per each Model 6310 Memory module
8M samples maximum total memory via 15 Memory modules
Total memory required for application = (S)(G)(C) where:
S = number of samples per memory segment
G = number of memory segments
C = number of active channels (1, 2 or 4)

Segmentation: Memory divided into segments; separate trigger for each segment, records only to end of segment for each trigger
Selectable pre-trigger/post-trigger percentage; percentage same for all segments on all channels
Dual timebase for each segment, same mode for all segments

Number of Segments: Selectable in binary increments from 1 to 1024

Segment Size: Selectable in binary increments from 1024 samples to the full memory length

Segment Record Rate: Sample rate divided by samples per segment 4880 segments/sec maximum (5MS/sec, 1024 sample segment)

Readout:
1. Entire active memory
2. Any active channel's memory
3. A memory section starting at any particular segment sample point (Offset command) and terminating at any other sample point in active channel memory (Abort command)

Readout Rate: 225 ksamples/second maximum via LeCroy 8901A IEEE-488 Interface

STATUS INDICATORS

LEDs: STATUS OK—Received valid setup command across bus
ARMED—Currently digitizing
TRIG'D—Trigger accepted and 6810 now digitizing post-trigger samples, if any selected

Module I.D.: Bus readable binary value "6810"

MECHANICAL

Packaging: R.F. shielding in conformance with IEEE-583 Standard (CAMAC)

MODULE	SIZE	HEIGHT	WIDTH	DEPTH
6810	4 slots	221 mm	68 mm	292 mm
6310	1 slot	221 mm	17 mm	292 mm

Power:

MODULE	+6V	−6V	+24V	−24V
6810	6A	3A	1.2A	1.2A
6310	1.7A	—	—	—

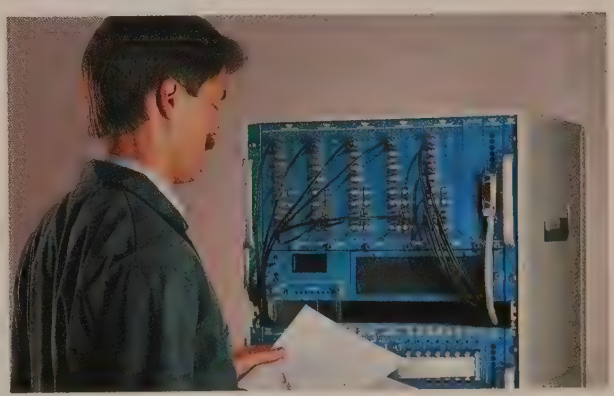
ENVIRONMENTAL

Operating Temperature: +15 to +35 degrees C (IEEE-583 instrument mainframe maximum exhaust temp. must be less than 50 degrees C)

Storage Temperature: −10 to +50 degrees C storage

Operating Humidity: 10% to 90% non-condensing

Operating Altitude: 0 to 10,000 feet above sea level



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AN INTRODUCTION TO THE 6810

The basic purpose of a transient recorder is to accurately sample an analog signal, digitize the samples, and write them to digital memory.

Many transient recorders provide only this basic function. They require external trigger generation and external amplification or attenuation of the signal of interest. If it is necessary to record the time between triggers, this also has to be done externally. The 6810 provides separately programmable conditioning of all input signals, very flexible triggering, trigger time interval recording and other features not often found in modular transient recorders. In one fully operational package it provides capabilities that usually require several modules and external cabling and configuration.

Below is a brief introduction to some advantages of using the 6810. Individual features are described in the following section. Details of individual features and how to use them are explained in the section titled "CAMAC command Details".

High Density, low cost

Up to five 6810s may receive power and program control in a standard 25-slot CAMAC instrument housing, providing up to 20 channels per instrument housing.

Flexibility

The 6810's multiple clock speeds, dual speed "priority" sampling, multiple trigger modes, programmable trigger source and level, and programmable sensitivity and offset for each channel provide the functionality of a programmable trigger generator, a gate and delay generator, a clock generator and one programmable amplifier per channel, all inside one module. The built-in recording of time intervals between triggers (with resolution to 1 μsec) can eliminate the need for external time to digital converters.

The 6810 may be programmed to use 1-channel sampling up to 5 megasample/sec, 2-channel sampling up to 2 megasample/sec, or 4-channel sampling up to 1 megasample/sec. Also, the flexibility inherent in a modular data acquisition system allows the 6810 and other types of modules to use the same instrument housing; the system may be reconfigured or expanded at any time.

High Resolution

The 6810 provides 12-bit resolution with excellent dynamic characteristics and better than 2% absolute accuracy.

Large, Expandable Waveform Memory

The 6810 includes a built-in 512K sample memory, expandable (with single-slot 6310 memory modules, 512K samples each) to 8 megasamples. Innovative packaging eliminates the need for external cables and ensures proper connection of external memories.

High Speed operation

The 6810 can acquire as little as 1024 samples per trigger. Up to 1024 triggers can be accepted before reading any data out. The 6810 loses no data between the end of one "segment" and the beginning of the next segment's pretrigger data. The "trigger dead

time" between the end of one record and the time the 6810 accepts the next trigger is only 160 μsec. Data can be read out at the full CAMAC speed, 1 megasample/sec (1.5 megabytes per second).

6810 Front-End Description

Figure 1 shows a highly simplified schematic of the 6810 input portion. Its purpose is to explain the input functions and to assist in making the proper connections and settings for the analog inputs. There are four similar channels, with channels 1 and 2 being different in that they are the only channels which can generate a trigger. One-channel operation is possible only on channel 1. Two-channel operation is possible only on channels 1 and 2.

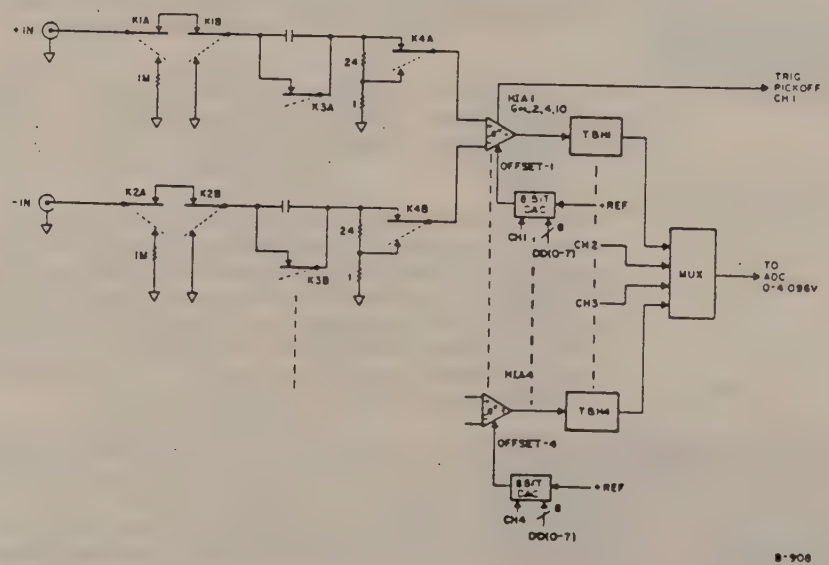


Figure 1 Front-End Block Diagram

Each channel is differential with plus and minus inputs on BNC connectors. The shells of the connectors are isolated from the front panel but are connected to analog ground on the signal conditioning board, which is connected to frame ground. Relays K1 and K2 control the input connections so the 6810 can be connected as:

1. Single-ended non-inverting.
2. Single-ended inverting.
3. Fully differential.

Relay K3 controls whether the input is AC or DC coupled. Relay K4 activates a 25 to 1 divider for the 10, 25, 50 and 100 V ranges.

With the relays as shown in Figure 1, the input is differentially direct coupled for the 0.4, 1, 2, and 4 V ranges (since the 6810 has a LSB of 100 μV, 1 mV, 2 mV and 4 mV respectively on these ranges, the actual full scale range is 0.4096, 1.024, 2.048 and 4.096 V). If relay K1 is thrown, the plus input to the HIA (Hybrid Instrumentation Amplifier) is grounded, and a 1 MΩ resistor is switched to the input so that the source always sees a 1 MΩ load. The input circuitry is now in the inverting condition. Similarly, if K1 is as shown and K2 is thrown, the negative input to the HIA is grounded and the input circuitry is in the non-inverting condition. With both relays as shown the input is fully differential.

The operation of K3 is to provide control for the coupling mode used for the input. As shown, the input is direct coupled when K3 is thrown, the input is AC coupled with a low-frequency 3 dB point of approximately 10 Hz.

K4 is shown for the input ranges of 0.4, 1, 2, and 4 V full scale. When it is thrown, a 25-to-1 divider attenuates the input for the 10, 25, 50 and 100 V ranges.

The HIA has digitally controlled gains of 10, 4, 2, and 1 so that the output of the HIA always has a range of 0 to 4.096 V. In order to accommodate bipolar, unipolar positive, and unipolar negative signals, each channel has an 8-bit offset DAC associated with it. For a bipolar input (symmetrical about zero) the DAC would be set to 128 (halfway in its range of 0 to 255). For unipolar positive signals it would be set at 0. And for unipolar negative signals it would be set at 255.

Each HIA feeds a unity gain Track-and-Hold, all of which are simultaneously sampled. The output of each Track-and-Hold go to an analog multiplexer (MUX) which feeds the high-speed 12-bit ADC on a separate board.

NORMAL OPERATING PROCEDURE

Power on the instrument housing. If the checksum of the setup information in the battery backed–up RAM is correct and the status information passes all the "verify" tests, the STATUS OK LED will come on and remain on. This means that the setup is the same one as used before power down and is valid. If the LED does not stay on, then the setup information is not the same as that last verified or used (the checksum is incorrect), or the verify tests failed.

It is possible to read the state of this LED from CAMAC, see the section "Verify Setup" for details.

NORMAL WRITE SEQUENCE

1. Set operations parameters – gains, offsets, clock speeds, number of active channels, etc. Optional: issue the VERIFY SETUP command **F(18) A(6)** to make sure the setup as programmed is acceptable. Read status byte to check result via CAMAC.
2. Send **F(9) A(0)** to arm the module. The 6810 will take several milliseconds to complete the arm sequence, during which time CAMAC lock out will be in effect. Optional: CAMAC I may be asserted to inhibit trigger prior to **F(9) A(0)** to several modules, then cleared to allow triggers to be recognized by the modules starting at the same moment.
3. Permit the module to accept the required number of triggers to fill the specified number of segments, or send **F(25) A(1)** to abort digitizing.

NORMAL READ SEQUENCE – LOGICAL READOUT

1. Before the first read, send **F(16) A(5)** W=readout "block" size and **F(16) A(6)** and **A(7)** to establish an offset in "blocks" from the beginning of the segment to the first word read out.
2. Send **F(18) A(channel #)** W=segment number, to indicate the desired channel and segment for readout.
3. Read out the trigger time interval for this segment using **F(2) A(1)**, if desired.
4. Read data using **F(2) A(0)**. Q=1 is returned on all cycles for which valid data are returned. **F(2) A(0)** cycles after the last valid word has been read return Q=0.

Notes: Step 1 need only be done once. Steps 3 and 4 may occur in any order.

BLOCK READ SEQUENCE

Block Read Data

Send **F(18) A(5)** to specify the starting address for readout as some multiple of 1024. *Note that the block readout size should previously have been set.*

Read with **F(2) A(0)**. Q=1 is returned for the number of words corresponding to the requested length. After the last datum corresponding to the requested length further **F(2) A(0)** cycles return Q=0.

Block Read Setup, Trigger Time Intervals or Stop Addresses

Send **F(18) A(0)**, **F(18) A(10)** or **F(18) A(11)** to enable block read of the appropriate item. (*Note: block read of setup may begin with any item and proceed for any number of items, as described in the "CAMAC Command Details" section.)*

Read with **F(2) A(1)** the desired length of data. Note that Q will always be 1. If the requested number of segments was not filled, then the time interval count and the stop address following the last valid segment will be set to maximum values (2^32–1 and 2^24–1, respectively).

OPERATING the 6810 with WAVEFORM-CATALYST

INTRODUCTION

The 6810 Waveform Recorder can be programmed via GPIB using an IBM PC XT, AT or strict compatible running WAVEFORM-CATALYST software (Versions 2.5 or later) connected to the Model 8901A or 6010 GPIB controller. WAVEFORM-CATALYST allows you to control 6810s or other modular instruments in up to 15 different instrument mainframes, giving you the capability to control 300 input channels when using 25-slot rackmount instrument mainframes.

WAVEFORM-CATALYST provides easy-to-learn single-keystroke commands which effectively turn your waveform recorder(s) and IBM PC into a digitizing oscilloscope. The WAVEFORM-CATALYST quick reference guide shown in Figure 2 diagrams the single keystroke commands. This manual will not attempt to explain more about the single keystroke commands or function libraries except in cases where their function is exclusive to the 6810 Waveform Recorder. For more information on the WAVEFORM-CATALYST functions, refer to the WAVEFORM-CATALYST user's manual. However, this manual will discuss in detail how to use the WAVEFORM-CATALYST Setup Menu to setup the 6810 measurement parameters.

RUNNING WAVEFORM-CATALYST

This manual will not address the hardware and software configurations needed on your computer to run WAVEFORM-CATALYST and the procedures for installing WAVEFORM-CATALYST on your system. This information is documented in the WAVEFORM-CATALYST user's manual shipped with the WAVEFORM-CATALYST software.

TRIGGER MODE COMMANDS

N Normal Trigger Automatically arms unit after a display or archive cycle, enabling acceptance of an external "hardware" or manual trigger

A Auto Trigger Causes a computer-generated stop trigger about two seconds after arming digitizer. Also will respond to a normal "hardware" trigger if received first

F Freeze Trigger Toggles between current trigger mode and disabled trigger, effectively freezing data when in Normal or Auto modes

S Single Trigger Arms digitizers for one trigger only

M Manual Trigger Generates a stop trigger when in Auto, Normal or Single Trigger mode.

H Average/Histogram Enters Average/Histogram mode. User chooses number of channels and sweeps to be processed. Same commands are used for both Model 8901A and 6010 control modules

B Begin Average Initiates start of averaging or histogramming acquisition after parameters are set in averaging menu.

Y Yes/No Test Waveform Limit Testing compares new data to predefined limits

TRACE CONTROL

1, 2, 3 or 4 Assign Trace Allows modules to be assigned to each of the four display traces, respectively

< or > Page Causes display to page left or right, respectively, by the current number of displayed points

D Define Origin Causes a new 8 ksample trace with the present location of the primary cursor becoming the display origin

J Join Blocks Connects 8 ksample blocks to display full memory length

= Set Page Displays desired data block

X Expand On/Off Toggles between the last expand setting and full + 8 ksample display

T Trace Restore Reads out battery backed-up memory from module

Keypad 3 Position Trace Initializes keypad "arrows" to allow shifting the horizontal or vertical position of the active trace

Z Zero Postion Returns to zero any horizontal or vertical trace position settings.

CURSOR CONTROL

Keypad 7 Primary Cursor Initializes keypad "arrows" to allow moving both the primary and secondary cursors horizontally (along same trace) or vertically (to activate new trace)

Keypad 9 Secondary Cursor Initializes keypad "arrows" to allow moving the secondary cursor horizontally (along same trace) or vertically (to activate new trace)

MODULE SETUP

L List Modules Lists all module types supported by system. Selection of one type provides display of parameter setup, plus prompt commands to edit current settings

E Edit Module Displays and allows the editing of parameters of single module defined by active trace. Right/left "arrows" select parameter to edit, up/down "arrows" activate next trace

U User definable CAMAC Commands Allows definition of up to nine direct "CNAF" control commands for almost any user supplied CAMAC module. Self-prompts allow Reading or Writing on disk or Listing on screen all nine settings, 1 to 9 displays specified setting with edit and execute commands

DISPLAY CONTROL

G Grid Format Provides choice of a Single, Dual or Quad grid array

O Grid On/Off Toggles between full grid or grid outline only

C Connect Points Toggles between just points or points connected by lines

Q Quick Draw Toggles between normal "anti aliasing" or quick-trace plotting

I Insert Text Allows user to insert text onto display screen, terminated by carriage return

COPY UTILITIES

W Write Data Allows writing data from a module or other internal data buffer to floppy or hard disk. Automatically prompts for file name, etc

R Read Data Allows reading a data file from floppy or hard disk to internal data display buffer. Automatically prompts for file name, etc

F2 General Purpose Disk Utilities Provides screen prompts for "Change Drive", "Directory", "Erase", "Re-name" and "Set Write Format" disk utilities

P Fast Print Screen Generates a fast Screen Dump to optional printer

PrtSc Print Screen Generates a larger Screen Dump to optional printer with the same aspect ratio as the screen (monochrome only)

FUNCTION KEYS

F1 Help Menu Shows definition of each key

F2 General Purpose Disk Utilities Provides screen prompts for "Change Drive", "Directory", "Erase", "Re-name" and "Set Write Format" general purpose disk utilities

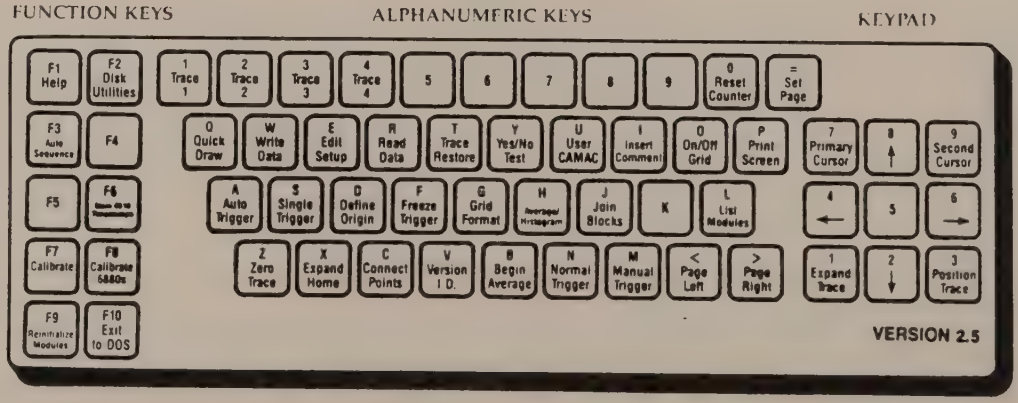
F3 Autosequence Mode Provides menu to learn or write sequence of CATALYST commands for later execution

F7 Calibrate Calibrates all modules with hardware self-calibration

F8 Calibrate 6880s Provides full or DC calibration of all 6880s

F9 Reinitiallze Modules to Default Settings.

F10 Exit to DOS



WAVEFORM-CATALYST Quick Reference Guide

Figure 2

6810 SETUP USING WAVEFORM-CATALYST

WAVEFORM-CATALYST Versions 2.5 and later include control software for the 6810 waveform recorder. Setup for the 6810 is controlled using the 6810 setup menu shown in Figure 3. To access the 6810 setup menu, press the **L**(ist Modules) key, press **[6]** and press **[Enter]**.

The 6810 setup menu shown in Figure 3 is the default (factory shipped) menu and is stored in the file named SD6810.CAT. If you would like to change the setup menu so that each time you run WAVEFORM-CATALYST and access the 6810 setup menu you receive your personalized 6810 menu, perform the following steps:

1. Modify the menu to fit your application.
2. Press the **[W]** key to write the file to disk.
3. When prompted with "enter filename:", type SD6810.CAT and press the **[Enter]** (or Return) key.

To make alternate 6810 setup menus, perform the 3 steps outlined above, changing the filename in step 3 to a filename of your choice. To read an alternate setup file, perform the following steps:

1. Press the **[R]** key to read the alternate file from disk.
2. When prompted with "enter filename:" type the filename of your alternate setup menu and press the **[Enter]** (or Return) key.

SETUP MODULE 6810

		A	B	C	D	E	F	G	H		J
1	NAME	A1	A2	A3	A4	B1	B2	B3	B4		
2	ACQUIRE	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
3	STORE	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
4	PROCESS	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
5	GPIB ADDR										
6	SLOT										
7	CHANNEL #	1	2	3	4	1	2	3	4	1	1
8	FULL SCALE V	2	2	2	2	2	2	2	2	2	2
9	OFFSET (%)	50	50	50	50	50	50	50	50	50	50
10	SEGMENT SIZE	8K	8K	8K	8K	8K	8K	8K	8K	8K	8K
11	PERIOD	.2us	.2us	.2us	.2us	.2us	.2us	.2us	.2us	.2us	.2us
12	EXT PERIOD										
13	COUPLING	+ DC	+ DC	+ DC	+ DC	+ DC	+ DC	+ DC	+ DC	+ DC	+ DC
14	SET TRIGGER	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
15	SET CLKMODE+?	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

All modules Enter Goto Help Next Previous Read Write
press space to return

WAVEFORM-CATALYST Setup Menu

Figure 3

Adding More 6810 Setup Capabilities

The setup menu shown in Figure 3 allows you to control two separate 6810 Waveform Recorders (not necessarily in the same instrument mainframe). However, if you need to control more than two 6810s you can add other 6810 setup menus using the WAVEFORM- CATALYST BUILDCAT utility.

Before starting, make sure you have the WAVEFORM-CATALYST Program and Library disks. You will also need IBM Professional Fortran Compiler FOR1 and FOR2 disks. To personalize the 10 modules listed in your "List Modules" menu, perform the following steps:

1. Make a subdirectory called BUILDCAT under the root directory and enter the BUILDCAT subdirectory by typing: MD \BUILDCAT CD \BUILDCAT
2. Place the WAVEFORM-CATALYST Program disk in Drive A of your PC and copy all the files into your subdirectory by typing COPY A:*.* C:\BUILDCAT. Repeat this process for all the WAVEFORM-CATALYST Library disks.
3. Place the IBM Professional Compiler FOR1 into Drive A and type COPY A:FOR1.EXE C:\BUILDCAT. Repeat this process for the FOR2 disk typing COPY A:FOR2.EXE C:\BUILDCAT
4. Type BUILDCAT.EXE and you will see a listing of all the modules supported by WAVEFORM-CATALYST. Follow all the directions on the screen, selecting up to 10 modules.
5. Compile DVMOD.FOR into DVMOD.OBJ using the Fortran compiler by typing FOR1 DVMOD. When the process is done running, type FOR2.EXE.
6. Run the IBM LINKER using LINKLIST as the automatic response file, by typing LINK @LINKLIST. LINKLIST automatically assumes that the executable program file will be placed in the subdirectory /PROG.
7. Copy DEFAULT.CAT, CATLST.EXE and the module type files (MTDxxxx.CAT, SDxxxx.CAT and DCxxxx.HPL where xxxx is the four character module identifier) onto the WAVEFORM-CATALYST Program Disk and/or into your CAT subdirectory if running WAVEFORM-CATALYST from your hard disk.

WAVEFORM-CATALYST Help Capabilities

WAVEFORM-CATALYST supplies a 6810 help screen which lists the important points to remember when using WAVEFORM-CATALYST to control your 6810. TO access the 6810 help screen(s), enter the 6810 setup menu shown in Figure 3 and press **[H]**. The 6810 help screen(s) text is shown in Figure 4.

6810 - 5 MHz Transient Recorder

12 bit resolution
1,2, or 4 channel operation
upto 8M memory

Notes:

1. IMPORTANT: In order to provide seperate menu entries for each channel's gain, offset and coupling each channel has its own column on the menu. The 'SLOT' for channel one should be the leftmost slot occupied by the module, the next SLOT should be specified for channel two, etc.
2. IMPORTANT: In order for CATALYST to correctly interpret the "Look At Me" signal from the module, the slot indicated by the "N" mark on the module must be assigned CHANNEL 3 on CATALYST's menu, CHANNEL 4 must be the next column on the right and CHANNEL 2 must be the column to the left. CATALYST checks these columns to see if we are in 4 or 2 channel mode; if neither says ACQUIRE YES then the module is in 1 channel mode. This means that the four channels of 6810 may NOT be split across menu pages.
3. All channel-independent settings (which is all but gain, offset and coupling) are set from the entries in the CHANNEL 1 column. The entries in the other channels' columns have no effect.
4. The number of words needed for each acquisition is: SEG SIZE x number of segments x number of active channels. Do not specify these items such that the acquired data will not fit in memory.
5. PERIOD: the minimum period is .2us with one channel active, .5 us with two channels active or 1us with 4 channels active. The 6810 will correct an attempt to pass these limits. CATALYST will annotate correctly.
6. The External clock is subject to the same restrictions as 3. above.
7. COUPLING: annotation '+ DC' means non-inverting input active, inverting input grounded, DC coupled; others are similar. 'GND ' means both inputs are grounded (DC coupled). Inputs present a 1Megohm impedance even when internally grounded.
8. Data is displayed in blocks of 4k words. Multiple blocks may be viewed simultaneously by assigning the module to more than one trace and paging to the desired blocks, or by using Join (see main help screen).
9. The last two menu items cause a series of questions to be asked when the the module's setup is updated. These items are neither initialized or updated until you answer these questions; the 6810 stores previous setup in its battery backed up setup memory. Answering a question by just pressing 'Enter' causes a default of no change in that setting, except for pretrigger holdoff which defaults to 'Yes'.
10. The 6810 manual discusses two aspects of 6810 behavior which might not be expected. The most noticable of these is that the first few samples of each segment are wraparound from the end of the segment. Please see the 6810 manual. CATALYST makes no attempt to compensate for these effects.
11. The f6 key saves time stamps to disk. The format of the file it creates is: bytes 0,1: time stamp resolution code (microseconds * 10**code)
    bytes 2,3: number of segments = number of time stamps
    bytes 4..7: First time stamp (arm to first trigger)
    etc. All values are low byte first.

6810 Help Screen Text

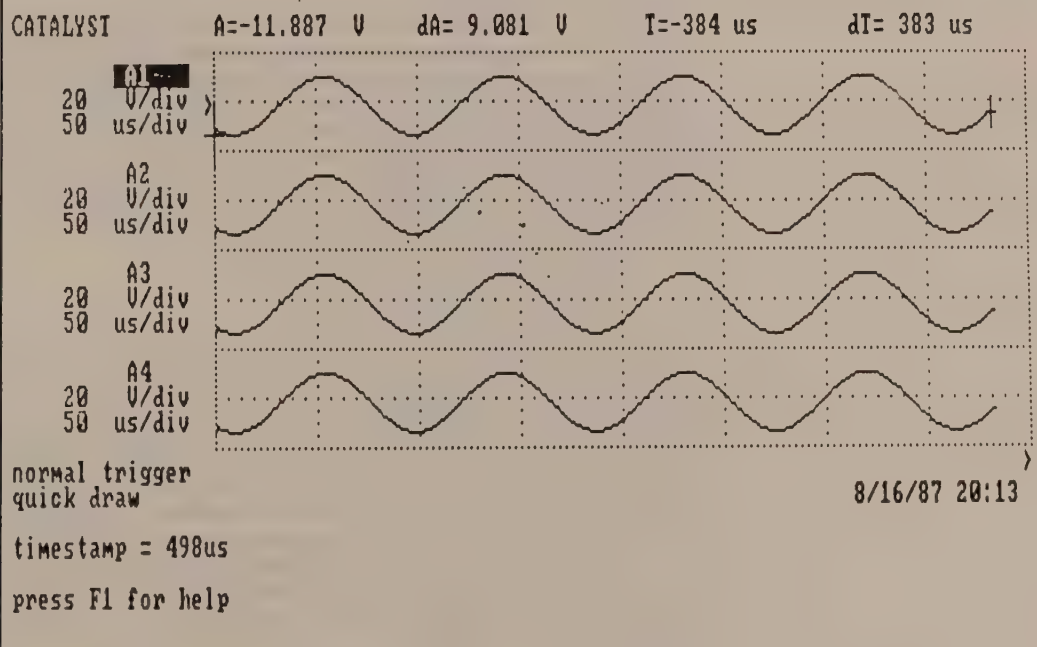
Figure 4

Individual 6810
Setup Parameters

In this section we will explain the function of the 15 setup parameters shown in the 6810's setup menu (See Figure 3). We will also provide the default setting, range of settings and the parameter's direct result on the 6810's operation.

NAME - Each 6810 measurement channels is named separately as shown in the first line of the 6810 setup menu. Default names are A1...A4 and B1...B4. The input channels can be named to any name not exceeding four characters. The name specified for the input channel will be displayed to the left of each displayed waveform as shown in Figure 5. To assign the first 6810 input channel to Trace 1 using the default name of A1 perform the following steps:

1. Type 1
2. Type A1
3. Press **[Enter]** (or Return)



6810 Channels Displayed Using Default Names

Figure 5

ACQUIRE - Each 6810 input channel is enabled by setting ACQUIRE to yes for that channel. Toggling between NO(the default setting) and YES is done by press the N(ext) key or the P(revious) key. The 6810 can be operated in the 1-Channel, 2-Channel and 4-Channel modes. To enable the 1-Channel mode,

set ACQUIRE to yes for Channel 1 only. To enable the 2-Channel mode, set ACQUIRE to YES for Channel 1 and 2. To enable the 4-Channel mode, set ACQUIRE to yes for all input channels.

NOTE: Setting ACQUIRE yes for Channels 1, 2 and 3 only will not enter the 6810 into 3-Channel mode. 3-Channel mode is not a supported 6810 feature and when the instrument is setup this way, it defaults to 2-Channel operation.

STORE - When the Store parameter is yes, the waveform for the applicable input channel is automatically copied to disk after each waveform update(when the waveform data is transferred to the computer). The waveform data files are stored in the \DATA subdirectory. The waveforms will be stored with incremental numeric filename extensions. For example, if Channel 1 (specified as A1) is triggered 3 times with STORE set to yes, the FILES A1.1, A1.2 and A1.3 are stored in the DATA subdirectory.

NOTE: The file extension numbers can be reset to 1 using the 0 (RESET COUNTER) key.

PROCESS - The PROCESS feature is advanced material and is intended for only people who are very experienced computer users or programmers. The parameter allows you to write your own code to process the displayed data. When PROCESS is enabled (=YES), a routine names "USER1" is called to process data each time it is read in from the specified input channel. Therefore, to use the PROCESS parameter, you must write the processing routine USER1. The calling sequence for USER1 is:

CALL USER1 (INBUF, DHDR, BLOCK)
Where INBUF is an 8 Kbyte data buffer
DHDR is a display parameter array
BLOCK is the current block number

Once the processing routine has been written and compiled, the object file must be copied to the object code link disk and the program should be relinked.

GPIB ADDRESS - Line 5 of the 6810 setup menu allows you to modify the GPIB address for your 6810. The 6810's GPIB address can be determined by checking the GPIB address switch on your instrument mainframe controller/interface module (models 8901A and 6010). Valid inputs for the GPIB address range from 1 to 15. Incrementing the GPIB address by 1 can be done by pressing the N(ext) key. Decrementing the GPIB address by 1 can be done by pressing the P(revious) key.

NOTE: All four channels of the 6810 must be specified with same GPIB address.

SLOT - In order for WAVEFORM-CATALYST to correctly interpret the "Look At Me" signal from the 6810 Waveform Recorder module, the slot indicated by the N on the 6810 front panel must be assigned to channel 3. Channel 1 is represented by N-2, channel 2 by N-1 and channel 4 by N+1. For example, if the 6810 N marker is in slot 8, the 6810 occupies slots 6, 7, 8 and 9 and should be assigned as the respective slots for channels 1 through 4.

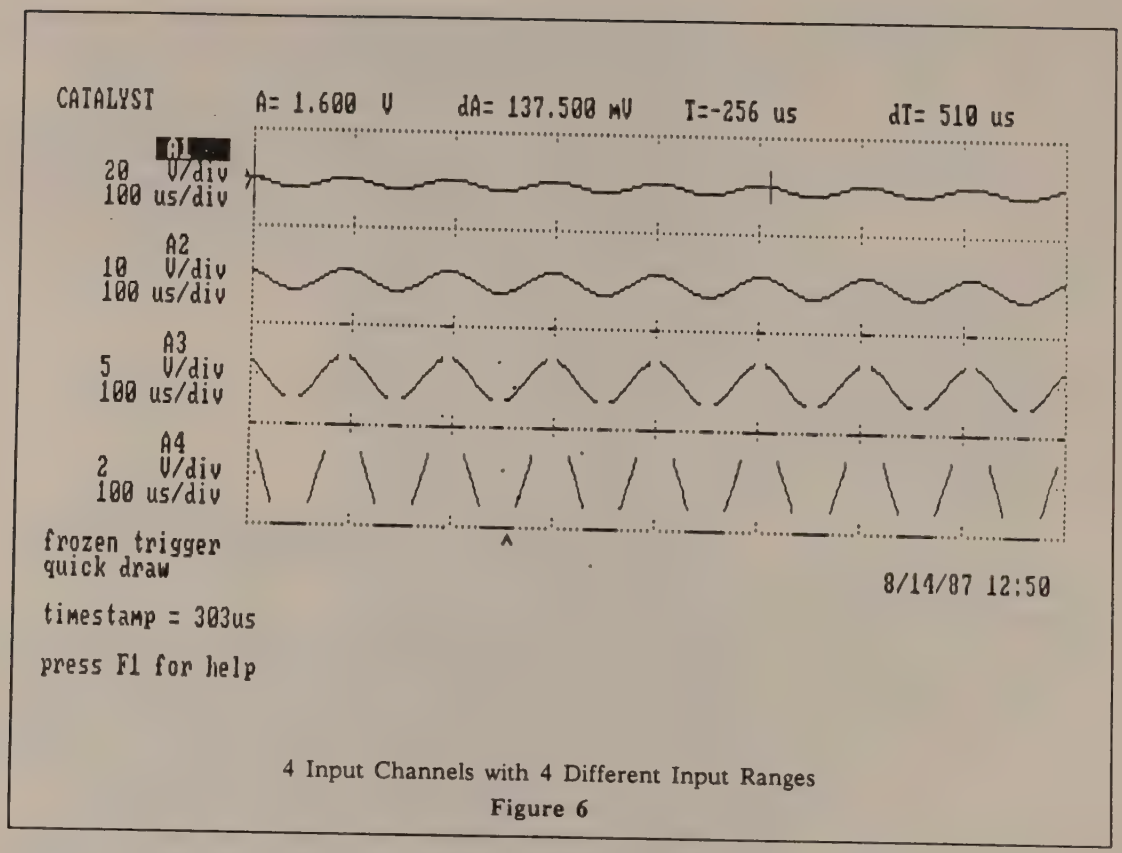
Channel # – The default settings for the channels is from left to right, 1 2 3 4. The order of these channels should never be changed are included in the setup menu only for reference.

FULL SCALE V – Line 8 in the 6810 setup menu allows you to modify the input full scale voltage range on a per channel basis. This allows different input ranges for each active channel. The default setting is 2 V full scale. A 2 V full scale input range for a channel allows a maximum of +1 V and a minimum of –1 V to be measured on that input channel. Valid input values for this parameter are:

400 mV
1 V
2 V
4 V
10 V
25 V
50 V
100 V

To increment through the valid voltage ranges, press the N(ext) key. To decrement through the valid voltage range press the P(revious) key.

When an input voltage range is set too high the magnitude of a measured signal may be smaller than necessary for viewing minute changes in the waveform's magnitude. To expand the signal vertically the display can be modified by pressing the 1 key (on the numeric key pad) to enter WAVEFORM–CATALYST into the EXPAND TRACE mode and then press the up arrow to expand the trace. The trace can also be expanded by retaking the measurement using an input voltage range which better approximates the peak–to–peak value of the measured waveform. Retaking the measurement is always the better alternative since expanding the display doesn't improve the vertical resolution(ability to see minute changes in the waveform's magnitude) like lowering the input voltage range. Figure 6 shows the same waveform measured using four different input voltage ranges. The 6810 provides excellent 12–bit vertical resolution. Take advantage of this accuracy by using the input voltage range which best approximates your waveform's magnitude.



4 Input Channels with 4 Different Input Ranges

Figure 6

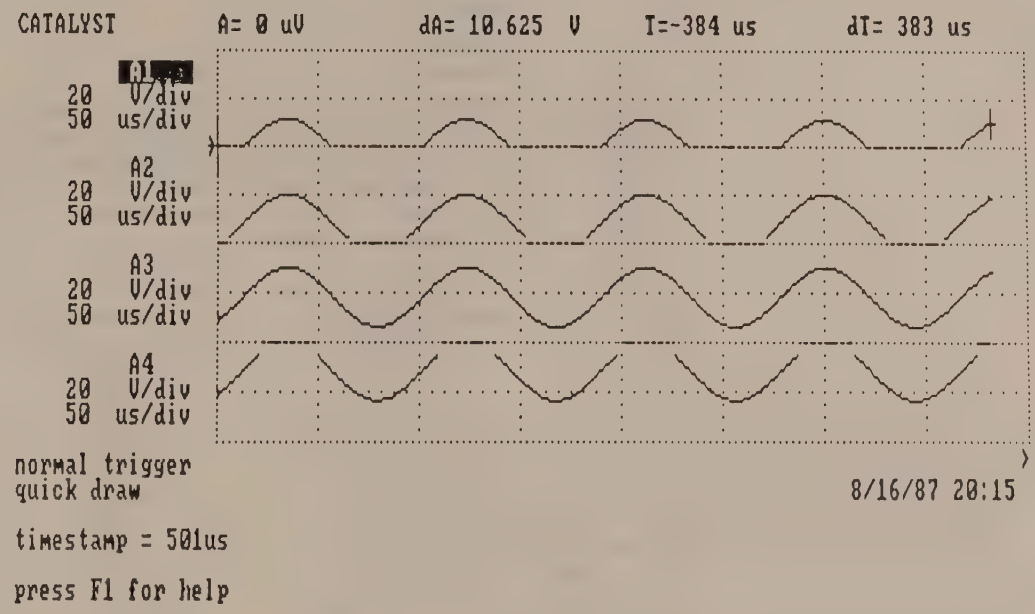
OFFSET – The DC offset introduced into your measured signal by the 6810 is expressed as a percentage of the input voltage range. Valid inputs for this parameter range from 0% to 100%. For example, if the input voltage range is set to 10 V full scale (giving the channel the capability of measuring voltages from −5 V to +5 V) the 0% to 100% range represents voltages in the −5 V to +5 V range with 50% always representing 0 V offset. In this case the following offset percentages represent the shown voltage levels:

100% --	+5 V Offset
75% --	+2.5 V Offset
50% --	0 V Offset
25% --	−2.5 V Offset
0% --	−5 V Offset

The offset percentage can be expressed differently for each of the four input channels. The default offset percentage is 50% (0 V offset) for all channels. Figure 7 shows the same waveform measured on all four input channels with the DC offset for each input channel set to a different value. To increment the offset

percentage, press the N(ext) key and to decrement the setting press the P(revious) key.

NOTE: The offset does not have to be reset when the input voltage range is modified. The offset percentage is always expressed as a percent of the current input voltage range and automatically updates with the input voltage range.



Same Waveform Measured Using Four Different Offsets

Figure 7

SEGMENT SIZE – The segment size allows you to control the number of samples that are stored in memory after each trigger event. The segment size is dependent upon the number of active (ACQUIRE = YES) channels (1, 2 or 4) and the number of segments recorded per channel. Each input channel must have the same segment size and the same number of segments. The segment size set for channel 1 is the segment size used for all active 6810 channels. The number of segments (programmable when SET CLKMODE+? is YES) for channel 1 is the number of segments used for all active channels. Segment sized can be set to the following values:

1 Ksamples
2 Ksamples
4 Ksamples
8 Ksamples – Default Setting

16 Ksamples
32 Ksamples
64 Ksamples
128 Ksamples
256 Ksamples
512 Ksamples
1 Msamples
2 Msamples
4 Msamples
8 Msamples

NOTE: Take special care to ensure that the 6810 setup is not configured to use more memory than is installed in your system. The maximum memory available depends on the number of 6310 Expansion Memory Modules connected to the 6810. The available memory depending on the number of connected 6310s is: # of Connected 6310s Amount of Memory

# of Connected 6310's	Amount of Memory
0	512K
1	1M
2	1.5M
3	2M
4	2.5M
5	3M
6	3.5M
7	4M
8	4.5M
9	5M
10	5.5M
11	6M
12	6.5M
13	7M
14	7.5M
15	8M

The maximum memory must always be less than or equal to the segment size times the number of segments times the number of active channels.

Period – Line 11 in the 6810 setup menu allows you to set the (f1) sample rate. The sample rate is the same for all four measurement channels. WAVEFORM-CATALYST uses the Period value from channel 1 for all active channels. Valid inputs for the Period parameter are:

PERIOD	Sample Rate
.2 μ sec	5 Ms/sec (Only one channel active)
.5 μ sec	2 Ms/sec (One or Two channels active
1 μ sec	1 Ms/sec
2 μ sec	500 Ks/sec
5 μ sec	200 Ks/sec
10 μ sec	100 Ks/sec
20 μ sec	50 Ks/sec
50 μ sec	20 Ks/sec
.1 msec	10 Ks/sec
.2 msec	5 Ks/sec
.5 msec	2 Ks/sec
1 msec	1 Ks/sec
2 msec	500 S/sec
5 msec	200 S/sec
10 msec	100 S/sec
20 msec	50 S/sec
50 msec	20 S/sec
EXT.	External Clock Enabled (see Line 12

The sample rate can be slowed by pressing the P(revious) key and speeded up by pressing the N(ext) key. The default sample Period is .2 μsec. When the Period is set to "EXT." make sure that the EXT PERIOD parameter (line 12) is set to approximate the frequency of the signal being input to the CLOCK IN connector on the 6810's front panel.

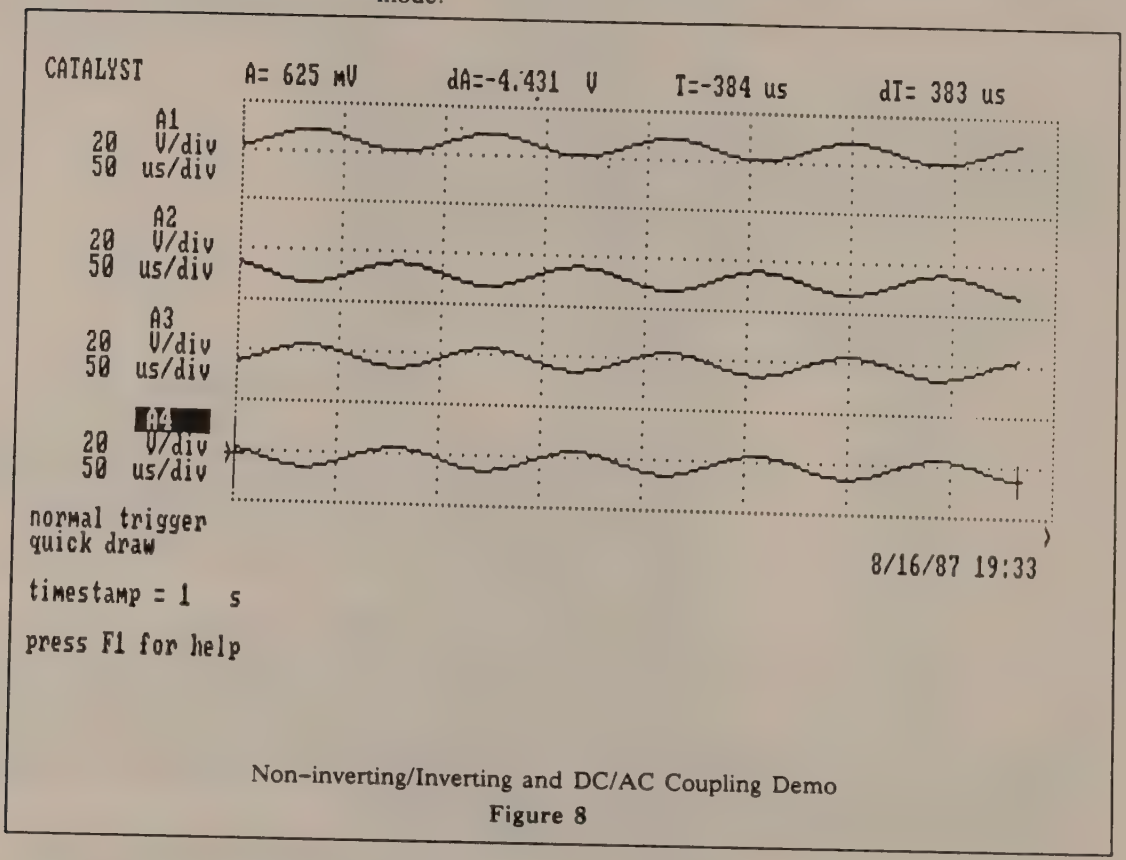
EXT PERIOD – The EXT PERIOD parameter in the 6810's setup menu allows you to enter the period of the external clock signal connected to the 6810's CLOCK IN connector. TO enter the 6810 into the External Clock mode, set the PERIOD parameter (line 11) in the "EXT." setting. The external clock signal must be a TTL signal of 5 MHz of slower and be connected to the CLOCK IN connector. Valid inputs for the EXT PERIOD parameter are periods of .2 μsec and larger.

COUPLING – The Coupling parameter allows you to set the coupling mode for the inverting and/or non-inverting input for each channel separately. Coupling modes are:

1. +DC (default) – Non-inverting DC coupled / inverting disabled
2. +AC – Non-inverting AC coupled / inverting disabled
3. -DC – Inverting DC coupled / Non-inverting disabled
4 -AC – Inverting AC coupled / Non-inverting disabled
5. d DC – Both inputs DC coupled
5. d AC – Both inputs AC coupled
6. GND – Both inputs disabled

Figure 8 shows the same signal measured on all four 6810 input channels. The signal has a DC offset for showing the difference

between AC and DC coupling. The signal measured on Channel 1 (A1) is measured using the non-inverting input in the DC coupled mode (notice how the DC offset from the signal source is apparent). The signal measured on Channel 2 (A2) is measured using the inverting input in the DC coupled mode. The signal measured on Channel 3 (A3) is measured using the non-inverting signal in the AC coupled mode. The signal measured on Channel 4 (A4) is measured using the inverting input in the AC coupled mode.



Non-inverting/Inverting and DC/AC Coupling Demo

Figure 8

SET TRIGGER – When SET TRIGGER is set to yes, WAVEFORM-CATALYST will ask the following questions upon exiting (when the space bar is pressed) the 6810 setup menu:

1. coupling (0=DC,1=ACHRF, 2=AC,3=ACLFR)?
2. slope (0=+,1=-,2=window,3=+h,4=-h)?
3. upper level (% full scale)?
4. lower level (% full scale)? – **not asked when slope=0 or 1**
5. source (0=ext, 1=chan1, 2=chan 2, 3=manual)
6. Delay (in eighths: -8 to 247)?
7. Trigger holdoff enable? (Y/N)

NOTE: Simply pressing the return key leaves the question/parameter unchanged from its last setting except for the Trigger Holdoff enable which defaults to YES.

Coupling – The Coupling parameter sets the type of coupling for the 6810's TRIGGER IN connector. The four coupling modes are:

0 – DC Coupling

1 – AC Coupling / High Frequency Reject (cutoff=6500 Hz)

2 – AC Coupling

3 – AC Coupling / Low Frequency Reject (cutoff=6500 Hz)

NOTE: If coupling is DC but the trigger source is an AC coupled input channel (channel 1 or 2), the trigger signal is AC coupled.

SLOPE – The five slope modes are:

0 – **Positive Slope** – The 6810 will trigger when a rising edge of the signal from the trigger source crosses the trigger threshold (upper level).

1 – **Negative Slope** – The 6810 will trigger when a falling edge of the signal from the trigger source crosses the trigger threshold (upper level).

2 – **Window Triggering** – The 6810 will trigger whenever the signal exits the window formed by the upper and lower trigger thresholds (upper and lower level respectively)

NOTE: Make sure that UPPER LEVEL > LOWER LEVEL.

3 – **Positive Hysteresis** – The 6810 will trigger whenever the signal passes completely through the region formed by the upper and lower levels. When operating in this mode, the lower level functions as a hysteresis threshold and generates a hysteresis event and arms the module when a falling edge of the signal crosses it. A trigger occurs when the signal continues through the region and crosses the trigger threshold (formed by the upper level). **A Hysteresis event must occur before each trigger event in order for the 6810 to trigger.** Hysteresis triggering allows you to discriminate between noise spikes and the signal when triggering on signals with large amounts of noise.

4 – **Negative Hysteresis** – The 6810 will trigger whenever of the signal passes completely through the region formed by the upper and lower levels. When operating in this mode, the upper level functions as a hysteresis threshold and generates a hysteresis event and arms the module when a rising edge of the signal crosses it. A trigger occurs when the signal continues through the region and crosses the trigger threshold (formed by the lower level). **A hysteresis event must occur before each trigger event in order for the 6810 to trigger.** Hysteresis triggering allows you to discriminate between noise spikes and the signal when triggering on signals with large amounts of noise.

UPPER LEVEL – The upper level is expressed as a percentage of the full scale trigger source (Channel 1, 2 or TRIGGER IN). Valid inputs are 0% to 100%. The upper level functions differently depending on the active slope mode:

> **Positive Slope (+)** – The upper level functions as a positive slope selective trigger threshold.

Negative Slope (–) – The upper level functions as a negative slope selective trigger threshold.

Window – The upper level functions as a positive slope selective trigger threshold. **Make sure that upper level > lower level.**

Positive Hysteresis (+h) – The upper level functions as a positive slope selective trigger threshold providing a hysteresis event has occurred on the lower level since the last trigger event.

Negative Hysteresis (–h) – The upper level functions as a positive slope selective hysteresis threshold.

LOWER LEVEL – The lower level is expressed as a percentage of the full scale trigger source (channel 1, 2 or TRIGGER IN). Valid inputs are 0% to 100%. The lower level functions differently depending on the active slope mode:

Positive Slope (+) – The lower level is not used in this mode and the user is not queried for its value.

Negative Slope (–) – The lower level is not used in this mode and the user is not queried for its value.

Window – The lower level functions as a negative slope selective trigger threshold. **Make sure that lower level < upper level.**

Positive Hysteresis (+h) – The lower level functions as a negative slope selective hysteresis threshold.

Negative Hysteresis (–h) – The lower level functions as a negative slope selective trigger threshold providing a hysteresis event has occurred on the upper level since the last trigger event.

SOURCE – There are four valid trigger sources:

0 = ext – TRIGGER IN signal used as trigger source.

1 = chan1 – Channel 1 Pickoff used as trigger source.

2 = chan2 – Channel 2 Pickoff used as trigger source.

3 = manual – All signal trigger sources (Channel 1, Channel 2 and TRIGGER IN) are disabled. 6810 can only be triggered manually.

DELAY – Trigger delay can best be described as two functions, Pre–/Post–trigger and true trigger delay. Pretrigger can be specified as –8/8 to 0/8 of the segment size. The trigger can be delayed from 1/8 to 247/8 of the segment size. To obtain the amount of time for the trigger delay you must multiply the fractional part used for the DELAY parameter times the segment length times the current sample period.

Trigger Holdoff enable?(Y/N) – Trigger holdoff enable allows you to disable trigger events that occur while recording data until reaching the end of the segment.

SET CLKMODE+? – When this function is set to yes, WAVEFORM– CATALYST will ask the following questions upon exiting (when the space bar is pressed) the 6810 setup menu:

1. dual clock mode(0–3)?
2. post–trigger near length? – Not asked if clock mode is 0
3. f2 sample period? – Not asked if clock mode is 0
4. Number of segments?
5. Time stamp res? (0=1 μsec,1=10 ,sec...4=10 msec):

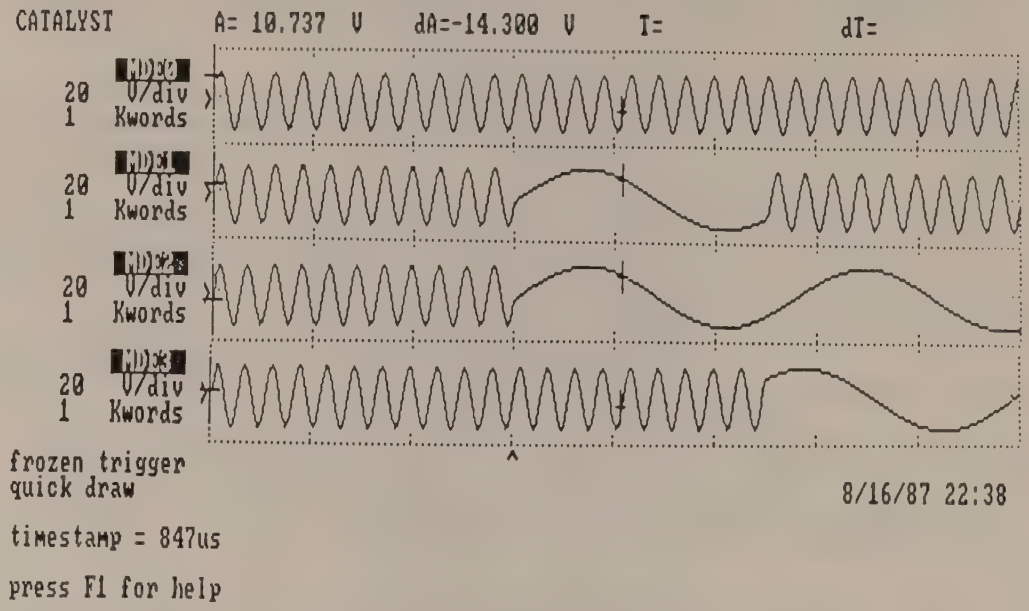
NOTE: Pressing only the return key without answering the asked question leaves that particular function unchanged from its previous state.

NOTE: The SET CLKMODE+? parameters for the channel 1 column apply to all four 6810 input channels. Channel 1 is the only channel that causes the question shown above to be asked when exiting the 6810 setup menu.

dual clock mode – The 6810 dual clock mode allows you to change the sample rate twice within the same waveform segment. The four dual clock modes are:

Mode	Pretrigger Data	Post–trigger Near Data	Post–trigger Far Data
0	Single Timebase	(f1)	for entire segment
1	f1	f2	f1
2	f1	f2	f2
3	f1	f1	f2

Figure 9 shows the same waveform measured in all four dual clock modes. The f1 sample rate (PERIOD) is 2us and the f2 sample rate is .2us. Pre–trigger data is contained in the first 3/8 (384 samples) of the segment. The Post–trigger near length is 320 samples.



Four Waveforms Measured Using All Dual Clock Modes

Figure 9

Post-trigger near length? – The post-trigger near length specifies the second timebase change point (the first change point being the trigger point). The post-trigger near length is expressed in samples after the trigger point and range from 1 sample to the segment length minus pre-trigger samples.

NOTE: The post trigger near length question is not presented when in dual clock mode 0.

f2 sample period – The f2 sample period is used (and asked by WAVEFORM CATALYST) only when operating in dual clock modes 1, 2 and 3. F2 can be greater than, less than or equal to f1 (specified by PERIOD in the main 6810 setup menu). Valid inputs for f2 are:

.2 µsec – (1 Active Channel only)
.5 µsec – (1 or 2 Active Channels only)
1 µsec
2 µsec
5 µsec
10 µsec
20 µsec
50 µsec
.1 msec
.2 msec
.5 msec
1 msec
2 msec
5 msec
10 msec
20 msec
50 msec

Number of segments – The number of segments can range from 1 to 1024. The number stored in the number of segments parameter is the number of trigger required after the arm command before data is read out to the remote computer. Each trigger will cause the recording of only one segment (for all active channels). The number of segments is the same for all active input channels. Make sure when setting the number of segments that you don't set the 6810 in a state which requires more memory than is configured and installed in the system. The number of segments times the segment length times the number of active channels must not exceed the total memory installed (using the 6310 Expansion Memory Module) in your system.

Time stamp res? (0=1 µsec,1=10 µsec...4=10 msec) – Valid time stamp resolutions are:

Entered Value	Time stamp Resolution	Maximum time (32 bits)
0	1 µsec	71.58 Minutes
1	10 µsec	11.93 Hours
2	100 µsec	4.97 Days
3	1 msec	49.71 Days
4	10 msec	> 16 Months

This parameter sets the minimum allowable time between counts when recording the time between valid triggers. The counter

records the time from the previous segment's trigger (or arm for the first segment's trigger) and saves the value in memory.

6810 CAMAC COMMAND SUMMARY

In order to facilitate independent control of each 6810 feature, each feature (for each channel, if appropriate) is set up by a different CAMAC command. Therefore, there are a large number of commands, but all are extremely straightforward.

Most of the 6810's setup is programmed by **F(16)** and **F(17)**, **A(0)** through **A(15)**. A few items are programmed by **F(19)**. Setup commands write the least significant eight CAMAC W lines directly into a battery backed-up memory which the 6810's microprocessor can read.

All setup items may be read back as a block or individually. For information about block read, see **F(18) A(0)**. Individual items are accessed by sending an F code sixteen less than the code used to write the desired item (to set up the address), then an **F(2) A(1)** to read the item. Successive **F(2) A(1)**s will read the following items in the same order as the block read.

F(18) contains mostly Prepare to Read commands. Please see the section "CAMAC Command Details" for further information about Prepare to Read commands. **F(2) A(0)** reads the time data. Other items (time stamps, stop addresses, setup) are read out by **F(2) A(1)**.

F(18) A(6) and **F(18) A(7)** are not Prepare to Read commands. **F(18) A(6)** causes a status byte to be generated which shows any reason a setup may not be acceptable, and attempts to fix the setup. This status byte may be read back. See the section "Verify Setup" and the description of **F(2) A(6)** in "CAMAC Command Details" for more information. **F(18) A(7)** causes several internal diagnostic tests to be run. Please see the section "CAMAC Command Details" for further information about this command.

CAMAC commands other than **F(16)**, **F(17)**, **F(18)** and **F(19)** directly control the digitizing hardware, i,e,; arm, trigger, or abort; control LAM, and read out data. These commands are listed at the end of this summary.

Note that F(9) A(0) (arm) and most of the Prepare to Read commands take longer than 1 μsec to complete. Most CAMAC commands are locked out during this time. Those that aren't are listed at the end of this summary. In the list below, those commands that take longer than 1 μsec to complete (and therefore cause CAMAC lock out) are marked with an asterisk. After one of these commands is sent, further CAMAC commands (except those noted below) are locked out until the 6810 is ready; they will have no effect and will return Q=0 if attempted during lock out. You may use F(11) A(0) to test whether the 6810 has locked out CAMAC.

Please see the section titled "CAMAC Command Details for more information on each command.

Write: **F(16)**; Set up for read back: **F(0) A**:

0 Time Stamp Resolution
1 Channel 1 Sensitivity
2 Channel 2 Sensitivity
3 Channel 3 Sensitivity
4 Channel 4 Sensitivity

5 "Block size" for data readout (use before first read)
6 Offset in "blocks" for "read channel #", low byte
7 Offset in "blocks" for "read channel #", high byte
8 Trigger Holdoff enable
9 Trigger Slope
10 Trigger Coupling
11 Trigger Level (upper level for window trigger)
12 Trigger Lower Level for window trigger
13 Trigger Source
14 Low byte, Post-trigger "near" number of samples
15 High byte, Post-trigger "near" number of samples

Write: **F(17)**; Set up for read back: **F(1) A**:

0 Number of Active Channels (= # words / sample)
1 Channel 1 Offset
2 Channel 2 Offset
3 Channel 3 Offset
4 Channel 4 Offset
5 Channel 1 source and coupling
6 Channel 2 source and coupling
7 Channel 3 source and coupling
8 Channel 4 source and coupling
9 Trigger delay
10 Number of samples per segment
11 Low byte, Number of segments
12 Hi byte, Number of segments
13 Dual Timebase Mode
14 F1 clock code
15 F2 clock code

Write: **F(18)**; (no read back on "prepare to read" commands) A:

0 Prepare to read setup
1 Prepare to read Channel 1 *
2 Prepare to read Channel 2 *
3 Prepare to read Channel 3 *
4 Prepare to read Channel 4 *
5 Prepare to block read from memory *
6 Verify Setup * / Set up for read of status = **F(2) A(6)**
7 Internal diagnostic tests *
10 Prepare to read trig address
11 Prepare to read trig times

Write: **F(19)**; Set up for read back: **F(3) A**:

1 Block write setup registers (See text!) (No read back)
2 Memory size

Other CAMAC commands:

		OK when CAMAC locked out?
F(2) A(0)	Block read data	Yes
F(2) A(1)	Block read registers	No
F(3) A(0)	ID	Yes
F(8) A(0)	Test LAM set and enabled	Yes
F(9) A(0)	Arm *	No
F(9) A(1)	Reset	Yes
F(10) A(0)	Clear LAM	Yes
F(11) A(0)	Test CAMAC lock out	Yes

F(24) A(0)	Disable LAM	Yes
F(25) A(0),A(1)	Trigger, Abort	Yes
F(26) A(0)	Enable LAM	Yes
F(27) A(0)	Test LAM set	Yes

• = *causes CAMAC lock out, see note above.*

Setup Commands

All commands listed in this section send setup information to the 6810. On each of these commands, the lower 8 bits of the W lines (write data) are saved by the 6810 in battery backed-up memory.

When the 6810 is armed, it first verifies that all setup is legal and attempts to correct illegal states. This action generates a status byte which may be read. Verify Setup is available as a separate CAMAC command which may be used at any time to generate this status byte. Please see the section titled "Verify Setup" for more information on this command.

Because of the internal architecture of the 6810 and the CAMAC requirement that the instrument take no irreversible action before S1 and have output ready by S1, reading back the setup is accomplished by two commands, one to set up the address inside the 6810 and the other to actually read out. All items written by **F(16)** are addressed by **F(0)**, and all items written by **F(17)** are addressed by **F(1)**. The memory size, programmed by **F(19) A(2)**, is addressed by **F(3) A(2)**. The item addressed is read out by **F(2) A(1)**. Successive **F(2) A(1)**s will read out the values which follow as described for **F(18) A(0)**, prepare to read setup, below. Unless the "verify setup" routine has run, the setup read back by **F(2) A(1)** will be exactly the bytes sent with the last corresponding **F(16)**, **F(17)** or **F(19)** command.

NOTE: In all cases below, the word "sample" refers to data from all active channels, which are sampled simultaneously.

This means that at a given sampling rate, a given number of samples takes the same time to acquire regardless of number of active channels. It also means that the number of words occupied by a segment is the number of samples multiplied by the number of active channels.

Below are the required settings on the W lines for each setup command. These settings are returned on the R lines when read back.

F(16) A(0): Time Stamp Resolution

W	Resolution	Maximum time (32 bits)
0	1 µsec	71.58 minutes
1	10 µsec	11.93 hours
2	100 µsec	4.97 days
3	1 msec	49.71 days
4	10 msec	over 16 months

This command sets the time per 'tic' of the counter recording the time between valid triggers. The counter's value recording the time from the previous segment's trigger (or arm, for the first segment) to this segment's trigger is saved for each segment.

These values may be block read or read individually with each segment; see "Prepare to Read" commands, below.

F(16) A(1 through 4) Channel n Sensitivity, n = 1 through 4

W	V/LSB	Full Scale p-p
0	100 µV	409.6 mV
1	250 µV	1.024 V
2	500 µV	2.048 V
3	1 mV	4.096 V
4	2.5 mV	10.24 V
5	6.25 mV	25.6 V
6	12.5 mV	51.2 V
7	25 mV	102.4 V

F(16) A(5): Block Read Length - length is 2^W * 1024 words
Examples: 0 = 1K, 1 = 2K, 2 = 4K, ... 13 = 8 megawords

This command must be used before the first **F(18) A(1..5)** command. For **F(18) A(5)**, prepare to block read, this setting only affects how many words can be read by **F(2) A(0)** before Q = 0 is returned. For **F(18) A(1..4)**, prepare to read channel #, the block length is used in conjunction with the next two CAMAC commands to determine the number of samples to skip before the first word read out. This command only has to be used once.

Note that it is always possible to abort a read sequence, see F(25) A(1) below. Also note that, like other settings, this setting is only brought into the microprocessor's memory from the battery backed-up CAMAC setup memory on arm F(9) A(0) or verify F(18) A(6). Changing this setting does have an effect until one of these commands is received.

F(16) A(6): Offset in blocks for 'read channel #', low byte
F(16) A(7): Offset in blocks for 'read channel #', high byte

Unlike any other setup commands, the 2 bytes entered by these commands are read directly from the battery backed-up setup memory every time a Read Channel n command is received. This 2 byte number, multiplied by the block size, gives the number of samples to skip before the first sample to be read out.

NOTE: if the offset is greater than or equal to the segment size, the offset is not applied.

These commands are useful for computers that must read the data in small blocks and have considerable overhead associated with reading each block. The readout offset may be used to skip hundreds of blocks, at a time cost of only two CAMAC cycles. If you plan to read data from start of segment, simply set these values to zero - no offset.

F(16) A(8): Trigger Holdoff enable

W	meaning
0	no holdoff
1	holdoff enabled

When enabled, triggers which occur while the specified length of pretrigger data are being collected are ignored. When disabled, a trigger occurring during the collection of pretrigger data would be

honored, so the segment would have less than the specified length of pretrigger data. The beginning of the pretrigger data will be distorted.

Note that the 6810 saves the address of the sample during which trigger was received (see the section "Dual Speed Clock Timing" for details). Also note that if the CAMAC trigger command F(25) A(0) is received while pretrigger data is being collected and holdoff is enabled, it is not ignored. Holdoff has no meaning if no pretrigger information is desired.

F(16) A(9): Trigger Slope

0 positive slope
1 negative slope
2 window trigger
3 positive slope trigger with hysteresis
4 negative slope trigger with hysteresis

If positive slope is set, the trigger "edge" occurs when the selected trigger signal rises through the trigger level set by **F(16) A(11)**. If negative slope is set, the trigger edge occurs when selected trigger signal falls through the level set by **F(16) A(11)**. The other trigger modes use both the trigger "upper" level, set by **F(16) A(11)**, and the trigger "lower" level, set by **F(16) A(12)**. If window trigger is selected, then the trigger edge occurs when the selected trigger signal either rises through the level set by **F(16) A(11)** or falls through the level set by **F(16) A(12)**. Therefore, window trigger can generate a trigger whenever the selected signal leaves the amplitude range between the two thresholds. The hysteresis trigger modes produce a trigger at either the upper or lower level as selected, but then will not accept another trigger until the signal has exceeded the other level. When the Arm command **F(9) A(0)** is received, the trigger circuitry is set in a state as if a trigger had just occurred. This ensures that the first trigger will be subject to hysteresis constraints, if any.

F(16) A(10): Trigger Coupling

0 DC
1 AC, high frequency reject
2 AC
3 AC, low frequency reject

The three dB point of both the low and high pass filters is approximately 6500 Hz.

F(16) A(11): Trigger "upper" Level (positive slope level for window trigger and hysteresis trigger modes; the only level used for simple positive or negative slope modes.)

W = 8-bit offset binary fraction of full scale setting (see **F(16) A(1 though 4)** above). When the trigger source is the External trigger input, W = an 8-bit fraction of +/- 5 V. Offset binary means W=0 is minus full scale, W=255 is plus full scale. See **F(16) A(9)** for information on how this level is used.

F(16) A(12): Trigger "lower" level (Negative slope trigger level for window trigger and hysteresis trigger modes). W = same as for **F(16) A(11)**. See **F(16) A(9)** for information on how this level is used.

F(16) A(13): Trigger Source

0 External trigger input
1 Channel 1
2 Channel 2
3 None (CAMAC trigger, F(25) A(0), only)

F(16) A(14): Low byte, Post-trigger "near" number of samples
F(16) A(15): High byte, Post-trigger "near" number of samples

These bytes must be set if dual timebase mode 1 or 3 is used. The number of post-trigger "near" samples may be 4 to 65535. Example: To select 300 samples Post-Trigger Near, send **F(16) A(14)** W(44) and **F(16) A(15)** W(1). See **F(17) A(13)**, below, for more information on the dual clock modes, and the section "Trigger and Dual Speed Clock Timing" for details on the timing of clock speed transitions.

F(17) A(0): Number of Active Channels

W	# channels	Maximum sampling speed
1	1	5 MHz
2	2	2 MHz
4	4	1 MHz

F(17) A(1 through 4): Channel n Offset, n = 1 through 4 W is an 8-bit offset binary fraction of 50% of the full scale p-p voltage, see **F(16) A(1 through 4)**. W = 128 means that the input range is symmetrically bipolar.

F(17) A(5): Channel 1 source and coupling
F(17) A(6): Channel 2 source and coupling
F(17) A(7): Channel 3 source and coupling
F(17) A(8): Channel 4 source and coupling

W Meaning
0 Non-inverting input, DC coupled.
1 Non-inverting input, AC coupled.
2 Inverting input, DC coupled.
3 Inverting input, AC coupled.
4 Double ended input, DC coupled.
5 Double ended input, AC coupled.
6 Both inputs internally grounded, DC coupled.
7 Both inputs internally grounded, AC coupled.

Double ended input means that both inverting and non-inverting inputs are active. Inputs present a 1 MΩ input impedance even when internally grounded.

F(17) A(9): Trigger delay

Number of eighths of a segment from trigger to the first sample in each segment. Any value of W will be valid. W is interpreted as ranging from -8 to +247. Values less than 0 give pretrigger data, values greater than 0 delay the trigger. Some valid examples are:

-8 All data is pretrigger. Recording in the segment stops at trigger.

-3 3/8ths of each segment pretrigger.

0 All post-trigger, recording starts at trigger.

+n After the trigger, the 6810 collects (n+8)/8

* segment length of data. The first n eighths are overwritten, so the earliest sample in each segment is delayed from the trigger by the number of sampling clocks necessary to fill n eighths of a segment.

F(17) A(10): Number of samples per segment

W	# samples/segment	W	#samples/segment
0	1K (1024)	7	128K (131072)
1	2K (2048)	8	256K (262144)
2	4K (4096)	9	512K (524288)
3	8K (8192)	10	1Meg (1048576)
4	16K (16384)	11	2Meg (2097152)
5	32K (32768)	12	4Meg (4194304)
6	64K (65536)	13	8Meg (8288608)

Note that a setting of 13 is possible only in one channel mode and 12 is possible in one or two channel mode. Please see the section "Verify Setup" for information concerning the checks applied to this setting.

F(17) A(11): Low byte, Number of segments
F(17) A(12): Hi byte, Number of segments

The number of segments may be set from 1 to 1024. This number of triggers will be required after each arm command; each trigger will cause the recording of a segment. The number of segments * samples/segment * number of active channels = total memory used per acquisition. Example: To collect 300 segments following each arm command, send **F(17) A(11)** W(44) and **F(17) A(12)** W(1). Please see the section "Verify Setup" for information concerning the checks applied to this setting.

F(17) A(13): Dual Timebase Mode

W	Pretrigger	Post-trigger "near"	Post-trigger "far"
0	----- single timebase at f1 -----		
1	f1	f2	f1
2	f1	f2	f2
3	f1	f1	f2

Each segment can be considered as three parts: pretrigger data, the first n samples of post-trigger data, and the rest of the post-trigger data. The dual timebase mode selects the sampling clock for each of these parts, as shown above. 0 means that all data is acquired using a single timebase, at the f1 clock. The other modes permit "importance" sampling. F1 and f2 may be any timebase.

See **F(16) A(14)** and **F(17) A(9)** for information on specifying the lengths of the three parts of each segment. Please see the section "Trigger and Dual Speed Clock Timing" for more information.

F(17) A(14): f1 sampling clock code

W	Rate	W	Rate
0	External clock	9	10 KHz
1	20 Hz	10	20 KHz
2	50 Hz	11	50 KHz
3	100 Hz	12	100 KHz
4	200 Hz	13	200 KHz
5	500 Hz	14	500 KHz
6	1 kHz	15	1 MHz
7	2 kHz	16	2 MHz – 2 ch only
8	5 kHz	17	5 MHz – 1 ch only

Note that the maximum permitted sampling clock depends on the number of active channels, see F(17) A(0). All active channels are sampled simultaneously at all speeds. If this setting is 0, all sampling is done at the external clock rate. The settings of the dual clock mode and the f2 clock rate have no effect.

F(17) A(15): f2 sampling clock code

Same coding as f1 (except 0 is invalid for f2), see **F(17) A(14)**. Note that in dual timebase modes f1 and f2 must not both be greater than or equal to 2 MHz.

F(18) A(7): Internal diagnostic tests. These tests are not system tests, but verify the lowest level of functionality of the digital controlling hardware. They thoroughly test microprocessor access to the dual-ported RAM which holds setup programmed from CAMAC, the microprocessor's internal RAM, and calculate a checksum of the control program ROM. This command takes several milliseconds to complete, please use **F(11) A(0)** to wait for completion. After this command executes, the following is true:

1. the setup is preserved.
2. the "STATUS OK" LED is on if the dual ported RAM tested OK; otherwise it is off.
3. Six F(2) A(1)'s may be issued to read the following result report: Bytes 1,2: Count of errors in dual ported RAM, high byte first. Byte 3: Pattern of errors in dual ported RAM. Any bit position in which an error ever occurred is set to "1" in this byte. Bytes 4,5: Checksum of program ROM, high byte first. Byte 6: Count of errors in the microprocessor's internal RAM. This count sticks at 255. NOTE: these bytes are stored into the dual-ported RAM to be made available over CAMAC. If the "STATUS OK" LED is not on after **F(18) A(7)** is executed, the dual ported RAM has errors and the values in these bytes may be compromised. Other dependencies: If the control program checksum is incorrect, all tests may be compromised. If the microprocessor's internal RAM has errors, the dual-ported RAM test results may be compromised – the test uses three bytes of the internal RAM. The ROM checksum and the internal RAM test do not use the internal or dual ported RAM, only the microprocessor's registers and, of course, the program ROM.

F(19) A(1): Block Write Setup, Registers. This command may be used after **F(18) A(0)** or any other command which can set up an

address for **F(2) A(1)**. It writes successive bytes into successive addresses less than 4096 in the dual-ported RAM in the Setup memory. Note that it is possible to write beyond the end of the setup information and eventually overwrite the stop trigger addresses using this command. (This might be useful for storing arbitrary bytes in the 6810's battery backed-up RAM, which could be read back by **F(2) A(1)**. This command does not provide any time savings when utilizing either the LeCroy 8901A or 6010 CAMAC controllers, but does simplify programming by permitting an array of setup values to be sent to the 6810 by single loop repeating this one command. **F(19) A(2)** Active Memory size W corresponds to the total active memory in units of 512K. Since 512K words of memory is built into the 6810, W is one greater than the number of 6310 memory modules attached, as follows:

W	Memory size
0	No checking (see explanation below)
1	512K (internal memory only)
2	1 megasamples
3	1.5 megasamples
4	2 megasamples
5	2.5 megasamples
6	3 megasamples
7	3.5 megasamples
8	4 megasamples
9	4.5 megasamples
10	5 megasamples
11	5.5 megasamples
12	6 megasamples
13	6.5 megasamples
14	7 megasamples
15	7.5 megasamples
16	8.0 megasamples

The 6810's microprocessor cannot sense how much memory is available. This command is available so that this information can be entered into the battery backed up memory as part of the setup. When the arm command **F(9) A(0)** is received, or when the Verify Setup command **F(18) A(6)** is received, the 6810 checks that the requested number of segments at the requested segment size will fit in the specified amount of memory. If not, the 6810 will force the number of segments (not the segment size) down to a number that will fit in the available memory. It also checks that at least one segment will fit in memory. If code 0 is specified for memory size, the 6810 never performs the checks described above. This permits the "arm" command to complete a few dozen microseconds faster.

Note: Verify Setup, F(18) A(6), is described in its own section, below.

PREPARE TO READ COMMANDS

All Prepare to Read commands, which set up to read digitized data, take longer than 1 μsec to complete. They are handled by the 6810's built-in microprocessor. After the command is sent, further CAMAC commands which require microprocessor service or attempt to access the battery backed up setup information are locked out until the 6810's microprocessor is busy; they will return Q=0 if attempted during lock out. You should use **F(11) A(0)** to test whether the 6810 has locked out CAMAC and wait for the completion of the Prepare to Read commands.

Data is read using **F(2) A(0)**. Q=1 is returned whenever valid data is returned. After the last sample has been read, further **F(2) A(0)** cycles return Q=0.

NOTE: DO NOT ISSUE F(2) A(0) to the 6810 AFTER ISSUING A 'PREPARE TO READ DIGITIZED DATA' COMMAND, UNTIL CAMAC LOCKOUT IS DEASSERTED (F(11) A(0) returns Q = 1).

NOTE: Prepare to Read Digitized Data commands are ignored when the main address counter is enabled because they would load a new address into the main address counter. The main address counter is enabled while digitizing and during data readout. Therefore, if you do not read all the data you asked for but want to send another Prepare to Read data command, you must issue the abort command first; see F(25) A(1) for details.

The commands Prepare to Read Setup, Trigger Times and Stop Addresses do not require microprocessor intervention. Therefore, they complete within one full speed CAMAC cycle. These commands load an appropriate address into counters which address the battery backed up memory where the items are stored. These items are read with **F(2) A(1)**, which increments the counters. Note that any setup command as well as intersegment service while digitizing loads a new address into these counters. F(2) A(1) would then read the byte last accessed. **F(2) A(1)** will always return data and Q=1; you must know how many bytes you want to read.

F(18) A(0) Prepare to Read Setup causes address 1 to be the next address read out of the setup memory. The bytes read by **F(2) A(1)** will be in the following order:

0 Time stamp resolution code
1 Channel 1 Sensitivity
2 Channel 2 Sensitivity
3 Channel 3 Sensitivity
4 Channel 4 Sensitivity
5 "Block size" for data readout
6 Offset for "read channel #", low byte
7 Offset for "read channel #", high byte
8 Trigger Holdoff enable
9 Trigger Slope
10 Trigger Coupling
11 Trigger level
12 Trigger low level for window trigger
13 Trigger source
14 Low byte, post-trigger "near" length
15 High byte, post-trigger "near" length

16 number of active channels
17 Channel 1 Offset
18 Channel 2 Offset
19 Channel 3 Offset
20 Channel 4 Offset
21 Channel 1 source and coupling
22 Channel 2 source and coupling
23 Channel 3 source and coupling
24 Channel 4 source and coupling
25 Trigger delay
26 number of samples per segment
27 Low byte, number of segments
28 High byte, number of segments
29 Dual timebase mode
30 f1 sampling clock code
31 f2 sampling clock code
32 Memory Size code
33 Status – error code from Verify Setup
34 Checksum – complement of sum mod 256 of preceding bytes.

35 State of "setup OK" and "armed" LED's. (0=both off, 16=status O.K., 32=armed, 48 = both on. Updated when these LED's change.)

36–41 Results from **F(18) A(7)**. Please see the description of that command, above.

If you read beyond this point, you will eventually reach the trigger addresses, stored starting at address 1024.

F(18): A(n = 1 through 4) Prepare to Read Channel n, segment W *(Note: upon receipt of this command, CAMAC is locked out. This command takes less than 2 msec to complete, whereupon CAMAC is re-enabled. You may then send F(2) A(0). You should wait for completion of this command using F(11) A(0).)* This command prepares to read out data of the channel specified on the A lines from the segment specified on the W lines. A may be 1 through 4, but should not exceed the number of channels which were active when the data was acquired. W may be 0 through 1023, but should not exceed the number of segments acquired. The 6810 calculates the address of the first sample to read out from the trigger address, the trigger delay, and the "readout offset" (see **F(16) A(5)**). After this command completes, **F(2) A(0)** will read the desired data and **F(2) A(1)** will read the 4-byte trigger time interval recorded for this segment; see **F(18) A(11)** for more information about the trigger time interval.

F(18) A(5): Prepare to read from specified address W = start address in 1 kilobyte blocks, i.e., if W = 8 then the next **F(2) A(0)** will read sample number 16384 from memory. NOTE: **F(16) A(5)** must be sent before this command is first used. (Note: upon receipt of this command, CAMAC is locked out. This command takes less than 500 μsec to complete, whereupon CAMAC is re-enabled. You may then send **F(2) A(0)**. You can wait for completion of this command using **F(11) A(0)**.) The layout of data memory is very simple. The first segment starts at address zero and ends at (segment length * number of channels) minus one. The second segment starts in the following byte and

ends at 2* (segment length * number of channels)- 1, etc. Within each segment, data for each sample is stored in consecutive words, channels 1 through the number active, in order. It will be necessary to read the trigger addresses to know where the trigger occurred within each segment since the trigger address may be anywhere within a segment. The trigger address shows the contents of the main address counters when trigger was recognized, but trigger is actually honored only on a four sample boundary (where the lowest 2 bits of the address are zero). Please see the section "trigger timing" for more information.

F(18) A(10): Prepare to read trigger addresses. Causes address 1024 to be the next address read out of the setup memory by **F(2) A(1)**. The trigger addresses are stored sequentially for each segment starting at this address in the battery backed up "setup" memory. Each is 3 bytes long. These values are the contents of the main address counters at the next End Of Conversion pulse after trigger was recognized. Each 3-byte value is read out, low byte first. Due to hardware constraints, the trigger is not necessarily honored at this instant; that is, the post-trigger sample count does not begin. The address at which trigger is honored can be determined from the trigger address. Please see the section "Trigger Timing" for more information.

If less than 1024 segments are acquired, 3 bytes of all ones are present after the last valid trigger address. Note that reading beyond the last valid trigger address does not get to the trigger time intervals, but wraps from address 4095 to 0.

F(18) A(11): Prepare to Read Trigger Time Intervals causes address 4096 to be the next address read out of the setup memory by **F(2) A(1)**. The trigger times are stored sequentially for each segment starting at this address in the battery backed-up "setup" memory. Each value is 4 bytes long. Each 4-byte value is the count of the time increments specified by **F(16) A(0)**between the previous segment's trigger and this segment's trigger, except the first 4-byte value is the time from arm to the first segment's trigger. Each 4-byte value is read low byte first. If less than 1024 segments are acquired, 4 bytes of all ones are present after the last valid trigger time interval.

Other CAMAC commands

F(2) A(0): Block Read Data. Returns 12 bits of data in the 12 least significant bits of the CAMAC dataway. Returns Q=1 when valid data is returned. An **F(18) A(1, 2, 3, 4 or 5)** command should precede the first **F(2) A(0)**. *WARNING: do not issue this command while digitizing. NOTE: readout of digitized data must either complete or be aborted. See F(25) A(1) below.*

F(2) A(1): Block Read Registers. Returns 1 byte of data in the 8 least significant bits of the CAMAC dataway. Returns Q=1 when valid data is returned. A setup command or **F(18) A(0, 10 or 11)** command should precede the first **F(2) A(1)**. Will not function while CAMAC is locked out; returns Q=0 in that case. *WARNING: do not issue this command while digitizing. NOTE: readout of registers never needs to be aborted.*

F(3) A(0): ID. Returns 12 bits of data in the least significant bits of the CAMAC dataway. The value of these 12 bits should be 6810.

F(8) A(0): Test LAM set and enabled. Returns Q=1 if the instrument is currently asserting LAM, otherwise returns Q=0.

F(9) A(0): Arm. Causes CAMAC lock out. This command causes the 6810 to read all CAMAC programmed setup from the dual ported RAM, "verify" the setup (see "Verify Setup", below), set up for acquisition and commence taking data. The time from decode of F(9) A(0) until the completion of this sequence is approximately 3.7 msec. The ARMED LED lights and CAMAC is re-enabled on the first sampling clock after the arm sequence is completed (note: if the LED does not light, you have selected "external sampling clock" and are not supplying one; see **F(9)A(1)** below).

After CAMAC is re-enabled, **F(25) A(1)** may be used to ABORT digitization on the next sampling clock.

F(9) A(1): Reset. Resets the 6810's microprocessor, disables the Main Address Counter, etc. After approximately 100 msec, the 6810 will "wake up" as if it had just been powered on. Any digitization or readout in progress is aborted.

F(10) A(0): Clear LAM.

F(11) A(0): Test if CAMAC lock out is in effect. Returns Q=1 if CAMAC lockout is NOT in effect, Q=0 if CAMAC access to the dual ported setup RAM is locked out.

F(24) A(0): Disable LAM Disables the assertion of LAM by this instrument on the CAMAC dataway. **F(8) A(0)** will still return Q=1 if LAM would be asserted if enabled.

F(25) A(0): Trigger. This command always simulates a valid trigger.

F(25) A(1): Abort. Disables the Main Address Counters, thus ending either digitization or readout of digitized data on the next clock. *NOTE: this means that to abort data readout, it is necessary to send one more F(2) A(0) after sending F(25) A(1).*

F(26) A(0): Enable LAM Enables assertion by this instrument of the Look-At-Me line on the CAMAC dataway. LAM is generated when acquisition is completed, that is, when the last segment to be acquired is completed.

F(27) A(0): Test LAM set. Returns Q=1 if the condition which could produce a LAM exists internally in the instrument, specifically, having completed digitizing normally. Otherwise, returns Q=0.

F(18) A(6): Verify setup. (Causes CAMAC lockout) Please see the separate section on this command, below.

F(2) A(6): Setup to read status from last Verify. After this, the next F(2) A(1) reads the status byte produced from the last "verify" of the setup, either due to **F(18) A(6)** or **F(9) A(0)**. *Note: F(18) A(6) also performs this action, i.e., it is not necessary to issue F(2) A(6) immediately after F(18) A(6) in order to read back the status byte.*

VERIFY SETUP

As previously discussed, the setup programmed from CAMAC is held in battery backed up RAM and is accessible from CAMAC at the full 1 MHz speed. Whenever this data is read out of the battery backed up RAM for use within the 6810, the setup is verified and any anomalies are corrected as described below.

There are only two CAMAC commands that cause verification to occur: VERIFY SETUP, **F(18) A(6)**, and ARM, **F(9) A(0)**. The corrected setup is written back to the battery backed up RAM so that it is accessible from CAMAC.

VERIFY SETUP has one non-obvious function: as soon as the setup is verified, the gain, offset and coupling settings are put into effect. This causes relay closures. Relays take several milliseconds to debounce. If VERIFY SETUP is not issued separately, the ARM command will cause these settings to go into effect about 4 milliseconds before sampling begins. Especially in the case where a switch from DC coupling to AC coupling is required, this may not be enough time to settle to 12 bit accuracy. It is therefore recommended that when these settings are changed the VERIFY SETUP command should be used.

VERIFY writes a status word and a checksum to the CAMAC accessible RAM along with the corrected setup. (At power on, the setup is read from battery backed up RAM and verified in order to set the STATUS O.K. LED, but only a byte reflecting the LED state is changed in the CAMAC accessible RAM; see the section titled "Normal Operation".) The checksum is the complement of the sum (modulo 256) of the bytes that preceded it. The status byte indicates what, if anything, was corrected by the verification routine. The bits in the status byte have the following meanings:

Bit 0: Illegal value – some item was set to a value which can never be valid.

Bit 1: Sampling clock speed set too high for number of active channels

Bit 2: Setup would have caused clock speed toggle between 5 and 2 MHz, which is impossible.

Bit 3: Post-trigger "near" number of samples exceeded the total post-trigger length.

Bit 4: Number of segments * number of samples per segment *number of channels exceeded programmed memory size.

Bit 5: Number of samples per segment * number of channels = # words of memory per segment exceeded memory size.

Bit 6: "Upper" and "Lower" trigger levels were reversed.

Bit 7: unassigned, always 0.

If several items were corrected, several bits in the status byte may be on.

At any time, **F(2) A(6)** may be issued to cause the next **F(2) A(1)** to read the status byte produced from the last "verify" of the setup, either due to **F(18) A(6)** or **F(9) A(0)**. Note: **F(18) A(6)** also performs this action, i.e., it is not necessary to issue **F(2) A(6)** immediately after **F(18) A(6)** in order to read back the status byte.

While verification is in progress the "SETUP O.K." LED on the 6810's front panel is illuminated and CAMAC is locked out. This

command takes between 3 and 3.5 msec to complete; you may wait for it using **F(11) A(0)**. When verification is completed, if the LED stays on, then the setup was correct as entered from CAMAC and has not been changed in any way. If the LED does not remain on, then something has been corrected. The status byte can be read to find out what corrections were necessary, if any. Of course, the complete setup can be read back to find which values were changed, however, it is probably easier to determine what was changed by reading the remainder of this section.

Note that once a setup is verified, it will pass all tests if verified again. Therefore, if VERIFY SETUP or ARM does not leave the SETUP OK led illuminated and you wish to read out the status byte, you must read it before issuing either VERIFY SETUP or ARM again or the status byte will be zero.

Verification performs the following checks in this order:

1. Check settings which range from 0 to something for out of range settings. If a setting is out of range, it is replaced with the default value. The checks are:

WHAT	MAXIMUM	DEFAULT - MEANING
Time stamp resolution	4	4 - 10 msec
Trigger slope	4	0 - Positive slope
Trigger coupling	3	2 - AC
Trigger source	3	0 - External Trigger
Samplers per segment	13	0 - 1024
Dual clock mode	3	0 - clock 1 only
Clock 1 frequency	17	14 - 500 kHz
Memory size	16	0 - No checking
Pre-trigger trig holdoff	1	1 - enabled
Gain, channels 1..4	7	4 - 10.24 V F.S.
Block Read size	12	2 - 4K samples
Coupling, channels 1..4	7	0 - (+) input, DC

Because the setup is held in battery backed up RAM, these tests will all be passed if each item has ever been set properly.

2. Number of active channels must be 1, 2, or 4; other settings are never valid. Default is next higher valid number of channels, except settings higher than 4 default to 4.
3. If clock 2 will be used (clock 1 is not set to external and clock mode is not set to 0 = clock 1 only) then check that clock 2 setting is between 1 and 17; other settings are never valid. If the clock 2 setting is invalid the dual clock mode is defaulted to clock 1 only.
4. Number of segments must be 1 to 1024. Other settings are never valid. Default is 1 segment.
5. If dual clock mode is 1 or 3 (so the clock speed is supposed to change after the first 'n' samples of post-trigger, called the post-trigger "near" length), check that the post-trigger "near" length is at least 4. Settings less than 4 are never valid. Default is 100.

6. Check that the segment size, which is specified in logical samples, multiplied by the number of words per logical sample (i.e., the number of active channels) is less than or equal to the memory size. If the memory size code is zero, the memory size is assumed to be 8 megawords. On error, segment size is defaulted to memory size.
7. If the dual clock mode is not 0 (both clocks will be used), check that clock 1 and clock 2 are not both either 2 MHz or 5 MHz and not the same. The 6810 cannot toggle between 2 MHz and 5 MHz. On error, the dual clock mode is defaulted to 0 = clock 1 only.
8. If the trigger slope/mode is window or hysteresis trigger, check that the "upper" trigger level is actually above or the same as the "lower" trigger level. If not, reverse them.
9. If the memory size code is not zero, check that the number of samples per segment * number of channels multiplied by the number of segments will fit in the programmed memory size. On error, the number of segments defaults to the maximum number that will fit.
10. Check that both clock 1 and clock 2 are less than or equal to the maximum clock speed available for the requested number of channels. Default for either is the maximum permitted clock speed for the requested number of channels.
11. Check that the post-trigger "near" number of samples is less than the total post-trigger length. If not, post-trigger near length is defaulted to total post-trigger length minus 64 samples.

After these checks, the "STATUS O.K." LED is extinguished if any bits in the status byte are on. The updated LED state is copied back to the battery backed up RAM together with the verified setup.

The primary purpose of the "verify" routine is to ensure that the 6810 cannot be put into an anomalous state. It also can be a convenience for the user in several ways, for example:

- If the number of segments is programmed as 1024, the maximum number of segments possible will always result (assuming that the memory size has been programmed).
- If the number of samples per segment code is programmed as 13 (8 megasamples), the maximum number of samples possible in one segment will always result (assuming that the memory size has been programmed).
- If either clock 1 or clock 2 or both are set to 5 MHz, the highest possible clock speed for the selected number of channels will always result.

TRIGGER AND DUAL SPEED CLOCK TIMING

Clock Timing

Parts I through III of this section cover aspects of the 6810's operation which are important to correctly interpret the timing relationship of the data read out.

The first three parts of this section do not attempt to explain the topics covered. The final part treats the same topics by explaining

the internal workings of the 6810. It may not be necessary to read the final part of this section.

The topics covered are:

Extra Post-Trigger Samples

Dual Speed Clock Switching

A. At Trigger
B. After "Post-Trigger Near"
C. At end of segment

Trigger Dead Time between segments

Detailed Theory of Operation

A. Trigger Time Interval and Address latching, Post-Trigger Counts
B. Dual Speed Clock Switching

Extra Post-Trigger Samples

Each segment acquired by the 6810 is actually a "circular buffer", that is, after it is entirely filled, the next sample overwrites the first sample, etc. "Trigger" commences the count of the number of post-trigger samples desired. After the appropriate number of post-trigger samples are acquired, the segment ends and the next sample is written to the first address in the next segment (if any). There are constraints imposed by our system, however, that restrict the address on which a segment can end. Because of these restrictions, up to ten extra words are written to the memory. (This worst-case is possible only in 5 MHz, one channel, multi-segment operation.) These extra post-trigger samples overwrite what would be the first pretrigger samples.

The logical readout commands, **F(18) A(1)** through **F(18) A(4)**, read out the data as if the number of pretrigger and post-trigger samples were precisely as requested. This is so the trigger address is at the desired position and the time relative to trigger may be calculated. Therefore the extra post-trigger samples appear as the first samples read out. This means that up to the first ten samples read out from each segment in 1-channel mode, or the first five samples in 2-channel mode, or the first two samples in 4-channel mode should be considered invalid.

Dual Speed Clock Switching

The clock can switch between f1 and f2 at three places: trigger, end of the first n samples of post-trigger, and end of the segment. Which two of these three points are enabled to cause a clock switch depends on the dual clock mode, set by **F(17) A(13)**. When a cause is disabled, no unusual timing occurs at that point. In dual clock mode 0, the clocks never switch and the 6810 behaves like any transient recorder.

You must remember that trigger is asynchronous to the sampling clock, so there is always a one sample uncertainty in the timing of the trigger relative to the previous or next sample. This is true for any sampled system. Because of this uncertainty it is best to avoid a clock switch at the event of interest and execute the clock switch either just before or just after the point of interest.

Therefore, a typical use of the dual-speed clock is capturing an event with a brief very fast beginning followed by a long "decay", such that the entire event is too long to be sampled at the high rate demanded by its beginning features. Dual clock mode 3 (pretrigger and first n samples of post-trigger at f1, the remainder of post-trigger at f2) would likely be used with f1 fast and f2 substantially slower. In this case the clocks switch after the first n samples of post-trigger and at the end of each segment. *Note: dual clock mode 3 does not switch clock speeds at trigger, allowing us to trigger on the event of interest.*

Dual clock modes 1 (f1-f2-f1) and 2 (f1-f2-f2) cause a clock switch at trigger. Therefore, it is best if the trigger precedes the event of interest in these cases.

The dual clock modes can be used freely to study data within each of the three pieces of each segment. The following information is presented for those who must attempt to calculate the time between events on opposite sides of a clock switch. As stated above, it is best to avoid such a situation when the highest timing accuracy is required.

Dual clock switching at trigger:

1) Switching from any speed 1 MHz or slower to 2 MHz or 5 MHz: The last cycle of the low speed clock is aborted and the high speed clock commences within a few hundred nanoseconds. For example, if there are "n" samples pretrigger, the time between all samples from number 0 to (n-1) is at the low speed clock; the time between sample n and n+1 and all after is at the high speed clock; and the time between sample (n-1) and n is an indeterminate period which will be less than that of the low speed clock.

(Note: The high speed clock should persist for a time at least equal to a half cycle of the low speed clock. For a more detailed explanation, read the last part of this section.)

2) Switching from any speed 1 MHz or slower to any other speed 1 MHz or slower: The clock period can be changed only at a transition. If the trigger address points to sample "n", then the time between samples 0 to n is at the first clock, the time between samples n+1 and all after is at the second clock, and the time between samples n and n+1 is either. The probability that the time from n to n+1 will be at the second clock is determined by the first clock (since there is a fixed time period at the end of each cycle where the trigger address can still be recorded but the clocks can no longer be switched); the probability is very high if the first clock is 20K or below. (The last part of this section contains a detailed discussion of this switch.)

3) Switching from 2 MHz or 5 MHz to any speed 1 MHz or slower: When the high speed clock is at a high level, the clock is switched to the low speed clock, which is assumed to be stopped at a high level, and the low speed clock is begun. (The assumption will always be met if the high speed clock has been selected for a time equal to or greater than a half cycle of the low speed clock.) The major effect to be aware of in this case is that the "pipeline" from clock generation to End Of Conversion is over

500 nsec. Therefore, one more 2 MHz clock or two more 5 MHz clock pulses are "in the pipe" and cannot be recalled when the switch occurs. For example, if the trigger address points to sample "n" and f1 = 5 MHz, then the time between samples 0 to n+2 is 200 nsec, the time between n+3 and all after is at the second clock, and the time between n+2 and n+3 is either. Please see the final part of this section if further details are required.

Dual clock switching after "post-trigger near": The one sample uncertainty of trigger relative to next sample also applies to this transition, since it occurs at a user specified number of samples post-trigger. However, since this transition can be predicted (that is, the PTN count is known), the pipeline effects mentioned above are compensated for automatically by the 6810. This will be reflected below.

1) Switching from any speed 1 MHz or slower to 2 MHz or 5 MHz As above, the last cycle of the low speed clock is aborted and the high speed clock commences within a few hundred nanoseconds. The abort comes when the signal Sampling Clock corresponding to the last PTN sample is counted. This is typically about 500 nsec after the start (rising edge) of the low speed clock cycle.

2) Switching from any speed 1 MHz or slower to any other speed 1 MHz or slower: As noted above, the decision to switch clocks is generated when the signal Sampling Clock corresponding to the last PTN sample is counted. This is typically about 500 nsec after the start (rising edge) of the low speed clock cycle. This cycle will complete, and clock cycles after that will be at the second clock speed. This means that the time between the last PTN sample and the next sample after that will still be determined by the first clock. (The last part of this section contains a detailed discussion of this switch.)

3) Switching 2 MHz or 5 MHz to any speed 1 MHz or slower: When the high speed clock is at a high level, the clock is switched to the low speed clock, which is assumed to be stopped at a high level, and the low speed clock is begun. (The assumption will always be met if the high speed clock has been selected for a time equal to or greater than a half cycle of the low speed clock.) For further details on the timing of this switch, please see the last part of this section.

Dual clock switching at end of segment: The clock switch at the end of segment always occurs during those few samples which are overwritten by the extra post-trigger samples discussed above. These samples should be ignored anyway, so this clock transition is of no concern.

Trigger Dead Time Between Segments

At the end of each segment, the 6810 must read and save the Trigger Address and the Trigger Time Interval for that segment. Trigger is inhibited until these actions are completed, about 160 microseconds. During this time the next segment's pretrigger data (if any) is being collected.

Details of Operation

This section describes details of handling triggers and switching the dual speed clocks (if enabled). The other causes of dual speed clock switching are also covered.

In the discussion below, the output of the timebase circuitry is referred to simply as "the clock". The clock goes to the sampling circuitry which returns "Sampling Clock". Sampling Clock is essentially the clock delayed by 350 nsec. Approximately 90 nec after Sampling Clock comes MEMCLK, which causes channel 1's data to be written to memory. MEMCLK lasts 60 nsec, and is immediately followed by EOC, End Of Conversion, which causes the address to memory to increment. Most counters in the system count EOC.

Trigger time interval and address latching, post-trigger counts: When a trigger condition is detected a latch is set. The output of this latch is called AST, for ASynchronous Trigger. AST causes a 100 nsec pulse to be generated which:

1) In dual clock modes 1 and 2, causes the decision to be made to switch from f1 to f2. The actual switch occurs some time later. A detailed description of the timing after making this decision to switch will follow.

2) Triggers the "post-trigger near" sample counter. This counter will now count positive going transitions of Sampling Clock. The "post-trigger near" counter will issue a pulse after the programmed count is reached which, in dual clock modes 1 and 3, will cause a switch from the current clock to the other clock.

3) Causes the current value of the 32 bit "time since last trigger" to be latched, and the counters to be loaded with zero. These counters count the number of microseconds (or longer intervals, as programmed) between triggers. The latched value is read and saved by the 6810's microprocessor at the end of each segment.

The pulse produced from AST lags AST by about 35 nsec. The LO signal, which indicates which clock, f1 or f2, should be used is valid within 90 nec of AST.

The signal AST also serves the following purposes:

1) At the next EOC after AST, the signal VALIDTRIG is produced. VALIDTRIG causes the address of the sample which has just been written to memory to be latched as the Trigger Address for this segment. The latched value is read and saved by the 6810's microprocessor at the end of each segment.

2) Due to hardware constraints, each segment must end on an address which is a multiple of four. Since the post-trigger

length is always a multiple of 128, the post-trigger count must begin at an address which is a multiple of four. VALIDTRIG is therefore gated with the lower two bits of the memory address bus. When these bits have the value "2", the next EOC enables the post-trigger counters, which have been held at zero; then the next EOC is the first word counted as post-trigger. This has no effect on when the clocks switch, if enabled; only on the total number of post-trigger samples.

From this information we can predict how many extra post-trigger (and therefore fewer pretrigger) samples are available, from the two least significant bits of the Trigger Address:

One channel mode Two LSB's of address	# of extra post-trigger samples
00	4
01	3
10	6
11	5

Two channel mode Two LSB's of address	# of extra post-trigger samples
00	2
01	1*
10	3
11	2*

Four channel mode Two LSB's of address	# of extra post-trigger samples
00	1
01	0*
10	1*
11	1*

*= trigger occured after sampling. The next channel data word is the first word in memory sampled after the trigger. The 6810 uses the stop address in this manner when the logical readout commands are used.

In fact, there are other concerns, such as pipelining of data flow, which can cause an extra couple of samples posttrigger. Since the memory stacks groups of four words to write to memory, up to four more words of memory (four samples in single channel mode, two samples in two channel mode, one sample in four channel mode) may be affected. At most speeds this will not occur, however; for example in single channel mode the number of extra post-trigger samples will match the predictions above for all speeds except 5 MHz.

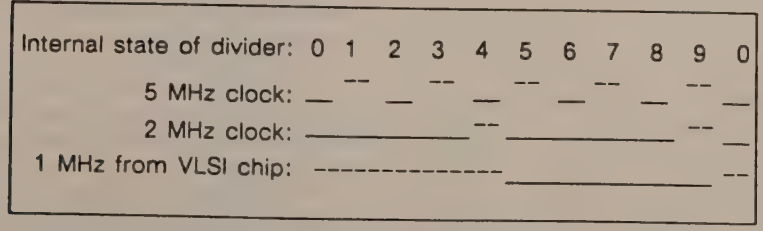
Because each segment behaves as a circular buffer, these "extra" post-trigger samples overwrite the first pre-trigger samples, as stated above. If a logical readout command (**F(18) A(1..4)**) is performed the readout is begun such that the trigger address is at the desired position in the segment so that time relative to trigger may be calculated. These extra samples therefore appear at the very beginning of the readout. This means that up to the first ten samples (worst case) read out by logical readout are actually these extra samples.

The post-trigger counters count rising edges of EOC. After the desired number of post-trigger samples, a signal is generated which causes the Memory Address Counters to jump to the beginning of the next segment after the next EOC. In dual clock modes 2 and 3 this signal also causes the decision to switch from f2 to f1 clock.

At the end of each segment, the 6810's microprocessor must read and save the Trigger Address and the Trigger Time Interval for the previous segment. While the microprocessor is busy the next segment's pre-trigger data (if any) is being collected. Trigger is inhibited until the microprocessor is finished, about 160 microseconds.

Dual speed clock switching: There are four facts which help explain the dual speed clock switching timing. (Understanding this material is not necessary to use the 6810).

- All clocks 1 MHz and below are created by a VLSI integrated circuit. It produces the low speed clocks by counting the required number of cycles of the 2 MHz clock and then changing the state of an output. On each transition the counter is loaded with the count to the next transition, ie, at each transition the time to the next transition is determined. This chip also contains the pre-trigger holdoff counter, the "post-trigger near" counter, and the two 16-bit counters which measure the trigger time interval.
- The 2 MHz and 5 MHz clocks are divided down from a 10 MHz crystal, absolute accuracy 0.01%. It is possible to switch from a clock produced by the VLSI chip to either of these or from either of these to the VLSI chip within 250 nanoseconds. The 250 nanosecond (max) delay is to meet set up and hold times of the VLSI chip.
- In dual clock mode 1 (only "post-trigger near" at f2), if f2 is 2 MHz or 5 MHz, it is important to specify enough posttrigger near samples to permit one half cycle of the low speed clock. This is because the switch from f1 to f2 occurs on trigger, which is asynchronous, so the state of the f1 clock is unknown. It is either already high, in which case it is immediately frozen; or it is low, in which case it will go high in a half cycle (at the most) and then be frozen. This permits the transition from f2 back to f1 to occur in a well defined manner, as discussed below.
- The 2 MHz and 5 MHz clocks are phase matched in the sense that a transition on the 2 MHz clock always corresponds precisely with a transition on the 5 MHz clock, as follows:



(Note: the VLSI chip clocks on the leading edge of the 2 MHz clock but typically has over 100 nsec propagation delay.)

Now let us consider the possible causes of a clock switch and the synchronization imposed at both low speed (1 MHz and below) and high speed (2 and 5 MHz) clocks.

1) Low speed to low speed. Transitions from low speed to low speed are constrained by the VLSI chip to occur only on an edge of the low speed clock. The 6810 attempts to further constrain the transition to occur only on a rising edge. Therefore, the clock should always complete a full cycle at one clock speed and then begin a full cycle of the new clock speed. In the diagram above, the transition may occur during the second half of any state except 3, 4, 8 or 9; this restriction is needed to provide adequate setup times for the VLSI chip and to wait for it to change state if it is going to. However, note that the "wait" is only 150 nsec. The worst case spec on this chip exceeds 150 nsec propagation delay. Below is an explanation of what will happen with a propagation delay in excess of 150 nsec. The excess will occur during the latter half of state 5 or state 0 in the diagram above. If the 6810 signals the VLSI chip to change clock speeds during this time (believing that the clock is low and not knowing that it is about to go high within nanoseconds), the transition will occur such that the first half of the cycle will be of a duration corresponding to one clock and the second half of the cycle will be of a duration corresponding to the second clock speed. Because trigger is asynchronous to sampling, the probability of this occurring at a clock speed transition due to trigger is at most .2 * (first clock speed / 1000000). The end of Post-Trigger Near is always detected about 500 ns after the beginning of the last PTN sample, so at this transition there is a certainty of this happening at speeds below 1 MHz. The probability when the first clock is 1 MHz depends on propagation delays through the VLSI chip.

2) Low Speed to High Speed. Both synchronous causes of clock switch will occur during the high (first) half cycle of the low speed clock (actually, about 500 nsec after the rising edge). Trigger may occur at any time. The actual clock switch occurs during the next 100 nsec interval that the selected high speed clock and the low speed clock are in the same state (either both high or both low), except during divider states 3,4 or 8,9 as shown in the diagram above due to setup and hold time requirements for the VLSI clock chip. The low speed clock counter continues to run until the state of the low speed clock is high. This is needed to switch back cleanly, as we will see below in the section "high speed to low speed". This means that the last cycle of the low speed clock is aborted at least 100 nsec prior to the next transition, and not more than 250 nsec after that request. The high speed clock commences at that point.

3) High Speed to Low Speed. The switch from high to low speed clock will always occur when the selected high speed clock is high. It is assumed that the low speed clock is high. At this time the counter that determines the time to the next transition of the low speed clock is reloaded, so the high state persists for the correct amount of time, i.e., the first cycle at the low speed clock is complete. *(Note: the first half cycle of the low speed clock will be "stretched" by up to 600 nS. This is the sum of*

propagation delay through the VLSI chip and the delay between the switch and the next 2 MHz clock, which the VLSI chip counts.)

The assumption that the low speed clock is at a high level is guaranteed valid only if the number of samples at the high speed clock correspond to a time equal to or greater than half a cycle of the low speed clock. If this assumption is not met a single short clock cycle may occur on this switch.

Because of the pipelining of data flow, one clock if 2 MHz or two clock pulses if 5 MHz are already "in the pipe" when the decision to switch is made; they cannot be recalled. This is visible if the switch from high to low speed occurs at trigger, as described above. If the switch from high to low speed occurs at the end of post-trigger near this effect is not visible because the 6810 automatically adjusts the requested Post-Trigger Near length to compensate for the extra sample(s) in the pipeline at the time of clock switch.

Changing the clock speeds over several orders of magnitude changes the duty cycle of the 6810's track and holds and A/D. It should be expected that this would result in a shift in DC offset. This shift can easily be characterized by setting source/coupling to 6 (= both inputs grounded, DC coupled) and taking data in the desired dual clock mode. Careful design has kept this shift at about one code (out of 4096) for most speed changes. The worst shift occurs when the clocks switch between 5 MHz and any clock below 50 KHz; in this case we have measured shifts on the order of 5 codes.

SERVICE DOCUMENTATION

PRODUCT ASSISTANCE Answers to questions concerning installation, calibration, and use of LeCroy equipment are available form the Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499, (914) 578-6059, or your field service office.

WARRANTY LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchase is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy will not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

SERVICE PROCEDURE Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned to the Customer Service Department,

a Return Authorization Number is required and may be obtained by contacting the Department at (914) 578-6059 or (914) 425-2000.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, the schematics may not agree in every detail with the accompanying product. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SPARE PARTS

The components used in LeCroy products are referenced on the supplied Replacement Parts List.

Replacement components are available from LeCroy for servicing LeCroy manufactured products. Please contact the Customer Service Department or local field service office and reference the LeCroy 9-digit part number.

PART NUMBER	DESCRIPTION	QUANTITY PER
103327103	CAP CERA MONO 50V .01 UF	95
103347155	CAP CERA MONO 50V 1.5 UF	4
103437104	CAP CERA MONO 100V .1 UF	3
116515241	CAP DIP MICA DM10 240 PF	1
116515390	CAP DIP MICA DM10 39 PF	1
116515680	CAP DIP MICA DM10 68 PF	1
142124476	CAP TANT DIP CASE 47 UF	11
142444107	CAP TANT DIP CASE 100 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	45
158849010	CAP VARIABLE 1 - 5 PF	1
161030000	RES COMP ZERO OHMS	1
161225101	RES CARBON FILM 100 OHMS	16
161225102	RES CARBON FILM 1 K	6
161225103	RES CARBON FILM 10 K	1
161225121	RES CARBON FILM 120 OHMS	1
161225200	RES CARBON FILM 20 OHMS	2
161225201	RES CARBON FILM 200 OHMS	2
161225301	RES CARBON FILM 300 OHMS	2
161225361	RES CARBON FILM 360 OHMS	3
161225470	RES CARBON FILM 47 OHMS	2
161225471	RES CARBON FILM 470 OHMS	9
161225512	RES CARBON FILM 5.1 K	1
161335101	RES CARBON FILM 100 OHMS	3
161335102	RES CARBON FILM 1 K	1
161335103	RES CARBON FILM 10 K	1
161335200	RES CARBON FILM 20 OHMS	1
161335273	RES CARBON FILM 27 K	1
161335330	RES CARBON FILM 33 OHMS	2
161335331	RES CARBON FILM 330 OHMS	1
161335510	RES CARBON FILM 51 OHMS	1
161335621	RES CARBON FILM 620 OHMS	1
168009256	RES PREC .1% 256 OHMS	1
168531265	RES PREC RN55D 46.4 OHMS	2
168531285	RES PREC RN55D 75.0 OHMS	1
168531297	RES PREC RN55D 100 OHMS	4
168531305	RES PREC RN55D 121 OHMS	6
168531360	RES PREC RN55D 453 OHMS	1
168531361	RES PREC RN55D 464 OHMS	1
168531373	RES PREC RN55D 619 OHMS	1
168531393	RES PREC RN55D 1.00 K	2
168531405	RES PREC RN55D 1.33 K	2
168531406	RES PREC RN55D 1.37 K	1
168531449	RES PREC RN55D 3.83 K	1
168531451	RES PREC RN55D 4.02 K	1
168531474	RES PREC RN55D 6.98 K	1
168531493	RES PREC RN55D 11.0 K	1
168531495	RES PREC RN55D 11.5 K	1
168531509	RES PREC RN55D 16.2 K	3
168531557	RES PREC RN55D 51.1 K	1
168531585	RES PREC RN55D 100 K	2
180247102	RES VARI CERMET 1 K	1
180247103	RES VARI CERMET 10 K	1
180247203	RES VARI CERMET 20 K	1
180247501	RES VARI CERMET 500 OHMS	1

PART NUMBER	DESCRIPTION	QUANTITY PER
190042471	RESISTOR NETWORK 470 OHMS	1
190642101	RESISTOR NETWORK 100 OHMS	2
190842101	RESISTOR NETWORK 100 OHMS	1
190842471	RESISTOR NETWORK 470 OHMS	9
200041186	IC D-TYP FLOP F10186PC	1
200071642	IC BUS TRANSCVR SN74LS642	2
200330002	IC 2-IN NOR GATE 74F02	1
200371374	IC D-TYP FLOP 74F374PC	2
204022002	IC HEX D M-S F-F MC10176L	2
204042002	IC NOR GATE MC10102P	1
204042003	IC LINE RECEIVER MC10115P	2
204042005	IC TYP D FL-FL MC10131P	2
204042008	IC QUAD TRANSL MC10125P	5
204042012	IC 2-IN AND GATE MC10104P	1
204042014	IC HEX AND GATE MC10197P	1
204042015	IC LINE RECEIVER MC10114P	1
204042016	IC 2-INPUT OR/NOR F10101P	4
204042103	IC 2-IN OR GATE MC10103P	4
205350472	IC PROM 512X8-BIT 74S472B	2
207249000	IC 6-BIT 75MHZ ADC AD9000SD	1
207251016	IC 8-BIT 30MHZ ADC CXA1016P	1
207281240	IC 12-BIT HI-SPEED DAC 1240	1
208111056	IC OP AMP JFET 1056	4
208122337	IC ADJ -VOLT REG LM337T	3
208211002	IC VOLT REF REF-02DP	1
208510317	IC ADJ +V REG 317LZ	1
208570317	IC ADJ +V REG LM317	2
208890581	IC PREC +10V REF 581	1
230110005	DIODE SWITCHING 1N4448	5
240225716	DIODE ZENER 12V 1N5242	1
253010835	DIODE HOT CARRIER HP2835	1
270110003	TRANSISTOR NPN 2N2222A	1
271170090	TRANSISTOR NPN UHF BFR90	2
275110001	TRANSISTOR PNP 2N2907A	1
280190531	TRANSISTOR "N" CH IRF531	2
290141200	DELAY LINE 200 NS	1
290142100	DELAY LINE 100 NS	2
300010001	BEAD SHIELDING FERRITE	2
300050001	CHOKE FERRITE SINGLE LEAD	13
402610001	CONN CO-AX PC MTG SMB	1
402610004	CONN CO-AX PC MTG SMB	1
405764007	SOCKET SINGLE WIRE CLOSED	8
433220002	FUSE PICO II 125V 3 AMP	2
433220003	FUSE PICO II 125V .5 AMP	2
453610026	CONN FLAT CABLE MALE 26	6
454310002	HDR DIP SOLD TO PC BD 2	5
454420032	HDR SOLD TAIL/FEM 32	5
500120002	TRANSIPAD "LARGE"	1
500860302	INSULATOR FOR TO-220	7
505070002	HEAT SINK FOR TO-220	7
574409005	WASHER SHOULDER NYLON #4	7
591692330	WIRE TEFLON TW PR AWG 30	2
592030026	CABLE FLAT AWG 28 26-COND	3
665034103	CER CAP W/SOLDER .01 UF	1

PART NUMBER	DESCRIPTION	QUANTITY PER
716810001	PC BD PREASS'Y 6810-1	1
HSA100	IC SUMMING AMPLIF HSA100	1
HTH100	HYB TRACK & HOLD	1

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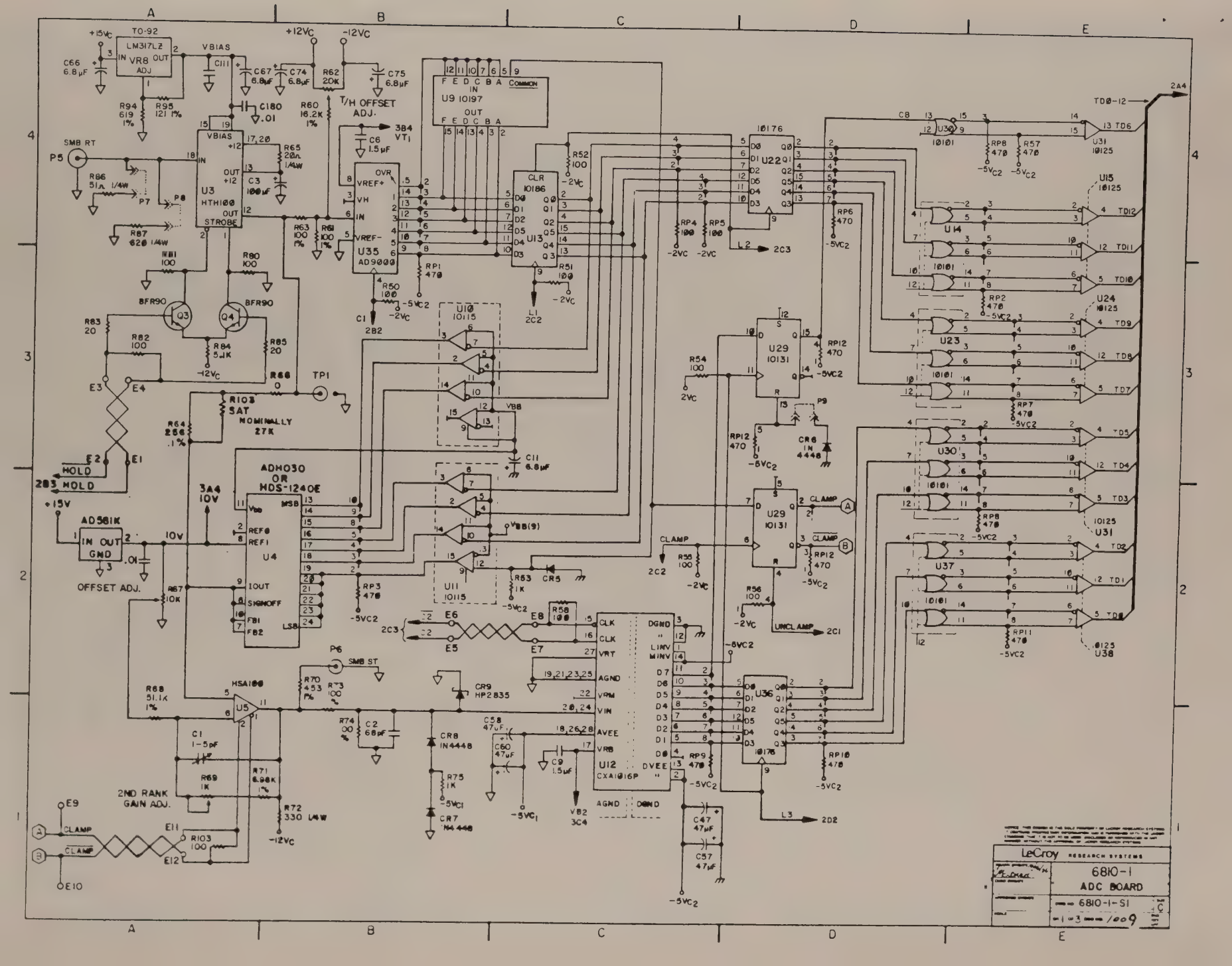
LeCroy RESEARCH SYSTEMS
6810-1
ADC BOARD
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ADH030 OR HDS-1240E
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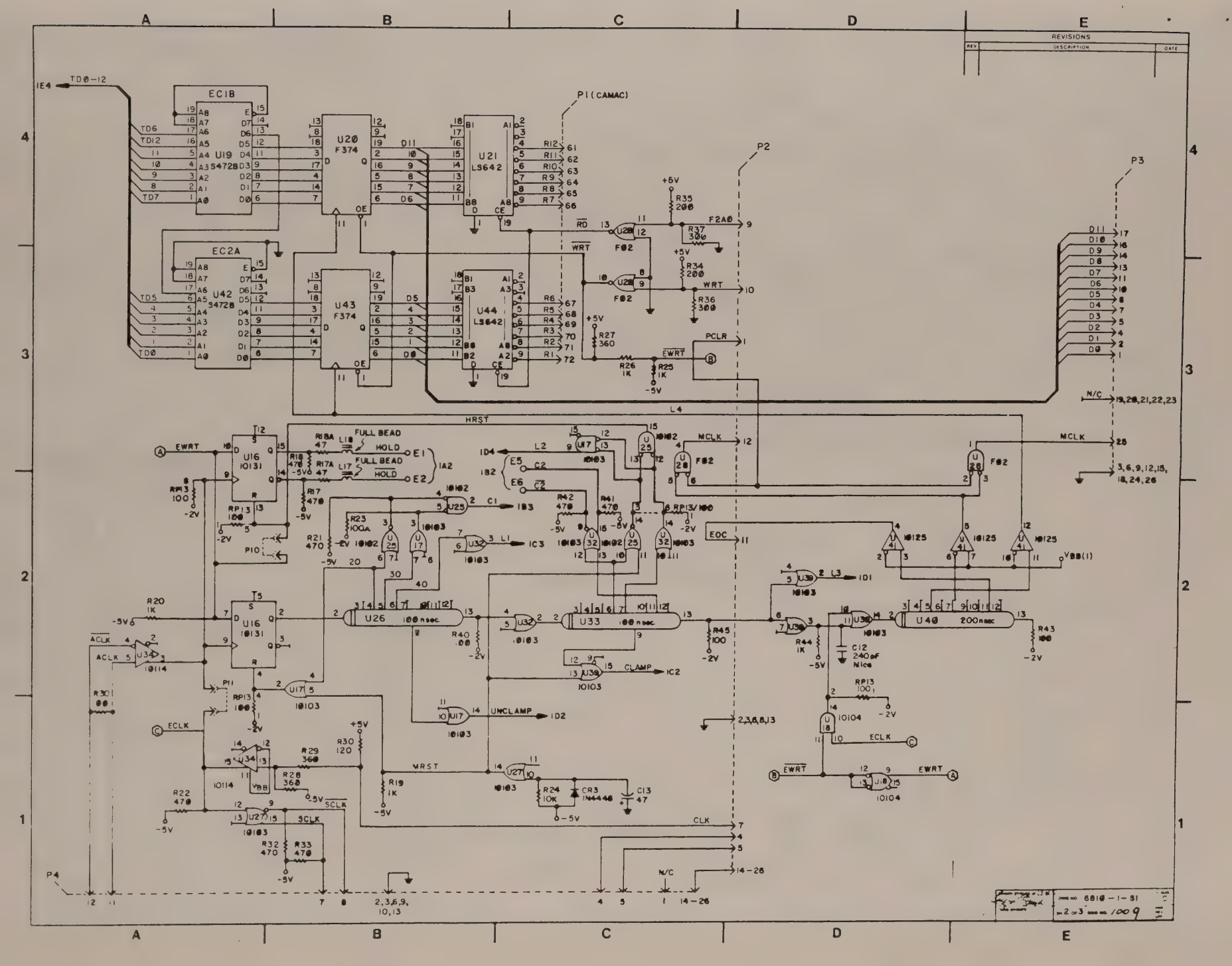
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-5V
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R37 300
R34 200
R36 300
R27 360
R26 1K
R25 1K
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U25
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U32
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U41 10125
U37
U36
U35
U30
U31
U29
U24
U22
U23
U3
U7
RP13 100
RP13 1001
R17A 47
R17B 47
R17 470
R18 470
R21 470
R23 100A
R42 470
R41 470
R20 1K
R40 100
R45 100
R43 100
R44 1K
R30 120
R29 360
R28 360
R22 470
R32 470
R33 470
R19 1K
R24 10K
CR3 1N4448
C13 47
C12 240pf Nilce
EOC
CLAMP
UNCLAMP
ACLK
ECLK
WRST
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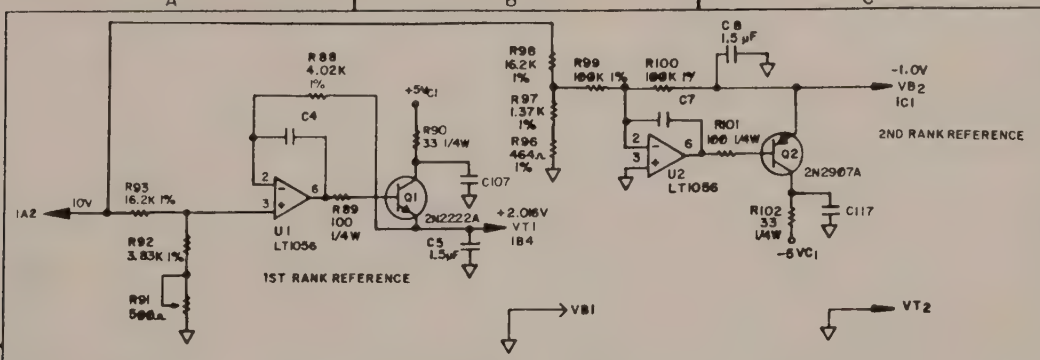
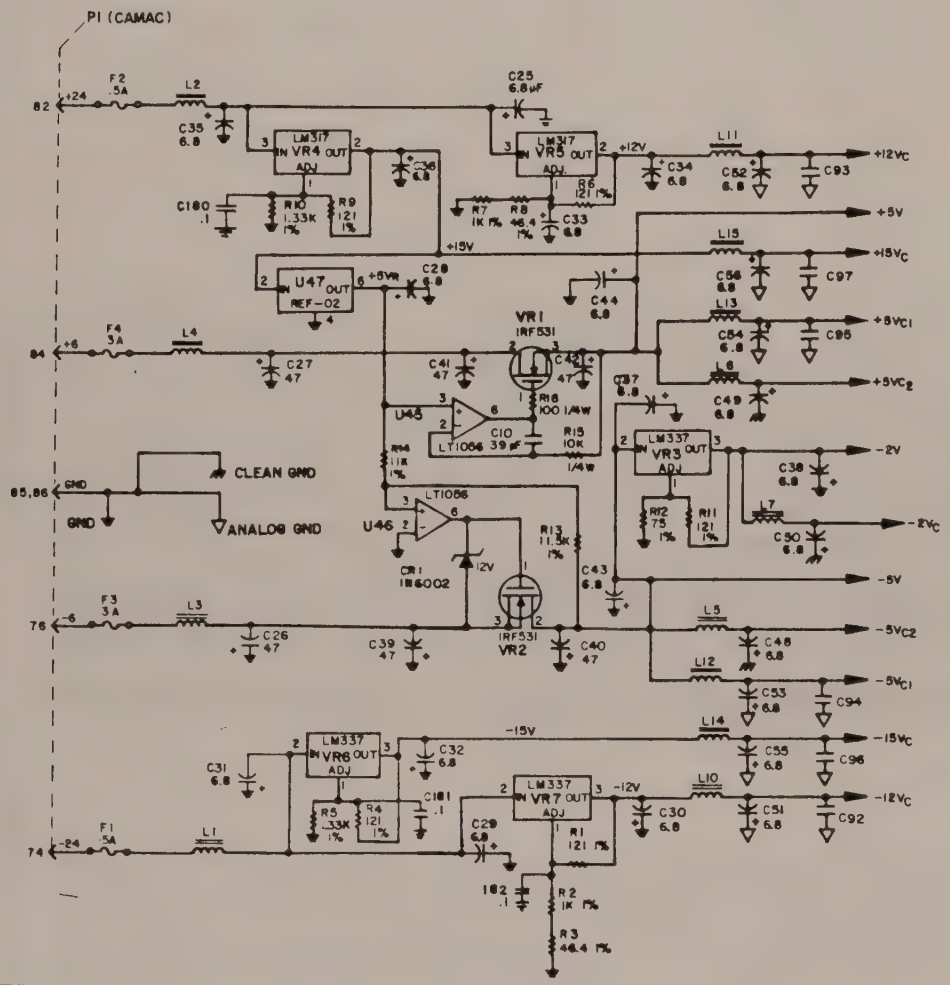




DEVICE	REF DESIGNATION	+15V C	+12VC	+5VC 1	+5V	-5V	-5VC 1	-5VC 2	-12VC	-15V C	AGND	EGND	GND
HTH100	U3	1	17,20	22	1		10	4,8		1	3,7,11 14,16,21 24		
AD9000	U35			7			1					2,16	
ADH030	U4	1								12	3,4,5		
10197	U9						8					1,16	
LT1056	U1,2	7								4			
LT1056	U45, 46	7								4			
10102	U25				8								1,16
10103	U17,27,32,39				8								1,16
10101	U14,23,30,37						8					1,16	
10114	U34				8								1,16
10115	U10, 11						8					1,16	
10125	U15, 24, 31, 38, 41				9	8							16
10131	U29						8					1,16	
	U16					8							1,16
10176	U22,36						8					1,16	
10186	U13						8					1,16	
74F374	U20,43				20								10
74S472B	U19,42				20								10
74LS642	U21,44				20								10
74F02	U28				14								7
200nS Delay	U40												1,14
100 nSec DELAY	U26, 33												1,14
REF02	U47	2											4
HSA100	U5		18	22			3	8			4,7,9, 10,12,13 14,15,16, 17,19,20 21		
10104	U18				8								1,16
CMOS8P	U12						18,1 2,25,13 26			1	19,21, 23,25	3,12	

U6, U7, U8, U18..... UNUSED

UNUSED DEVICES		
10101	U14	9,13,18
	U23	9,13,18
	U37	9,13,18
10103	U27	4,5,2;6,7,3
10125	U15	13,14,18
	U24	13,14,18
	U38	13,14,18
	U41	13,14,18
10114	U34	9,10,6,7
10104	U18	4,5,2;6,7,3

NOTE: ALL NON-VALUED CAPACITORS ARE 0µF, CERAMIC.

LAST REFERENCE DESIGNATION USED

L	C	RP	-	J	CR	TP	-	-	MP	P	J
47	103	13	2	5	9	3	4	5	8	11	1

NOTE UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%

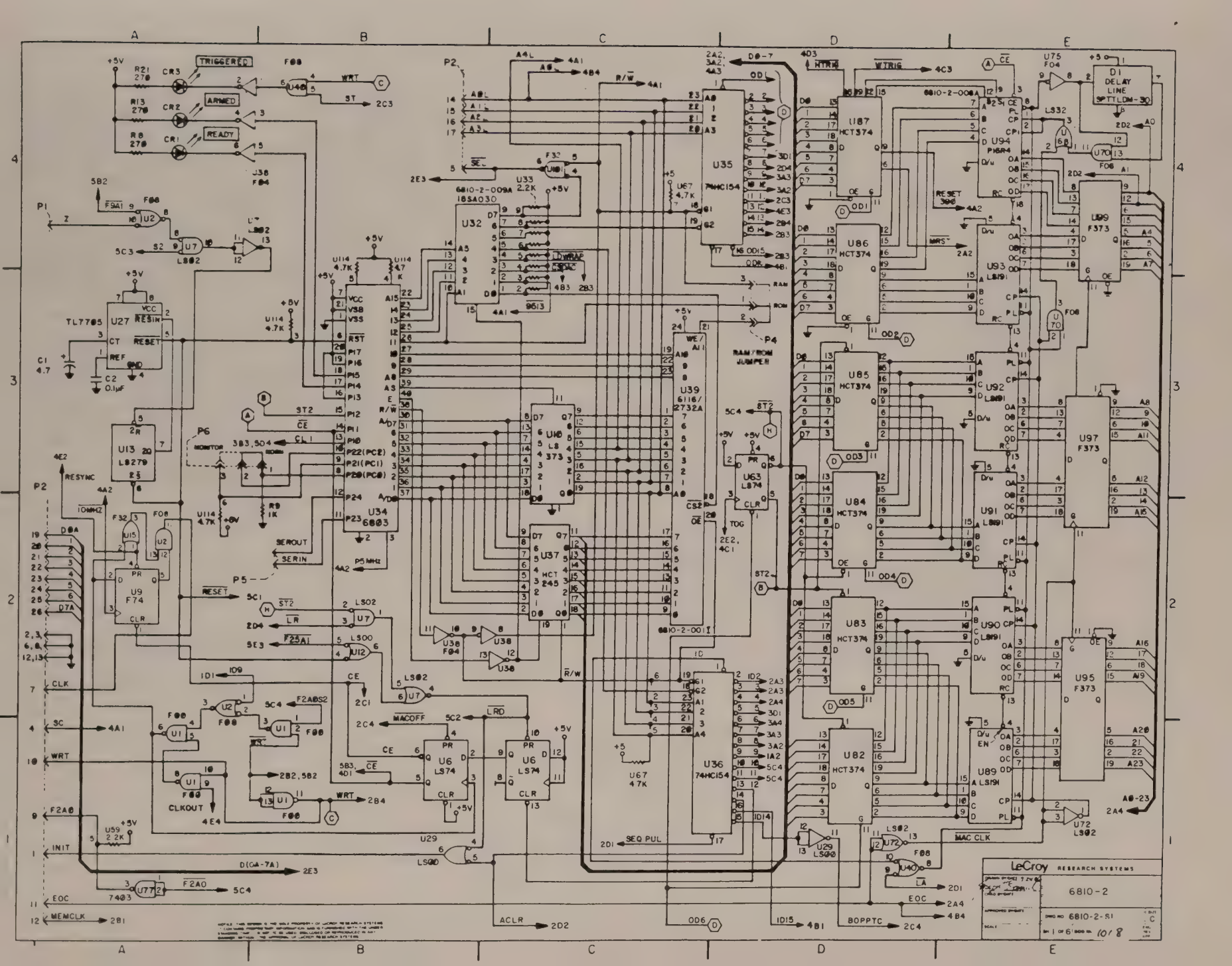
6810-1-81

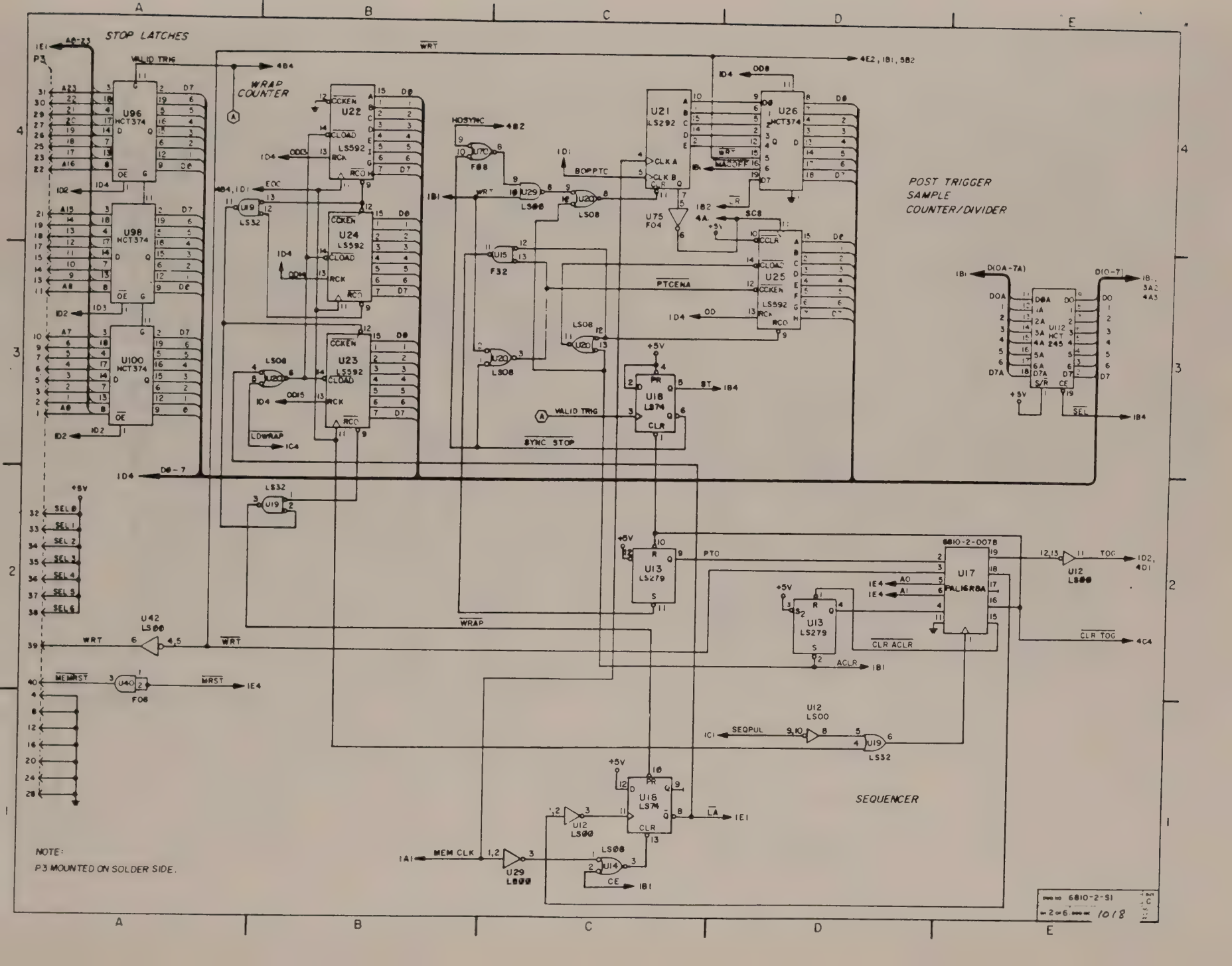
-3-3 mm 1009

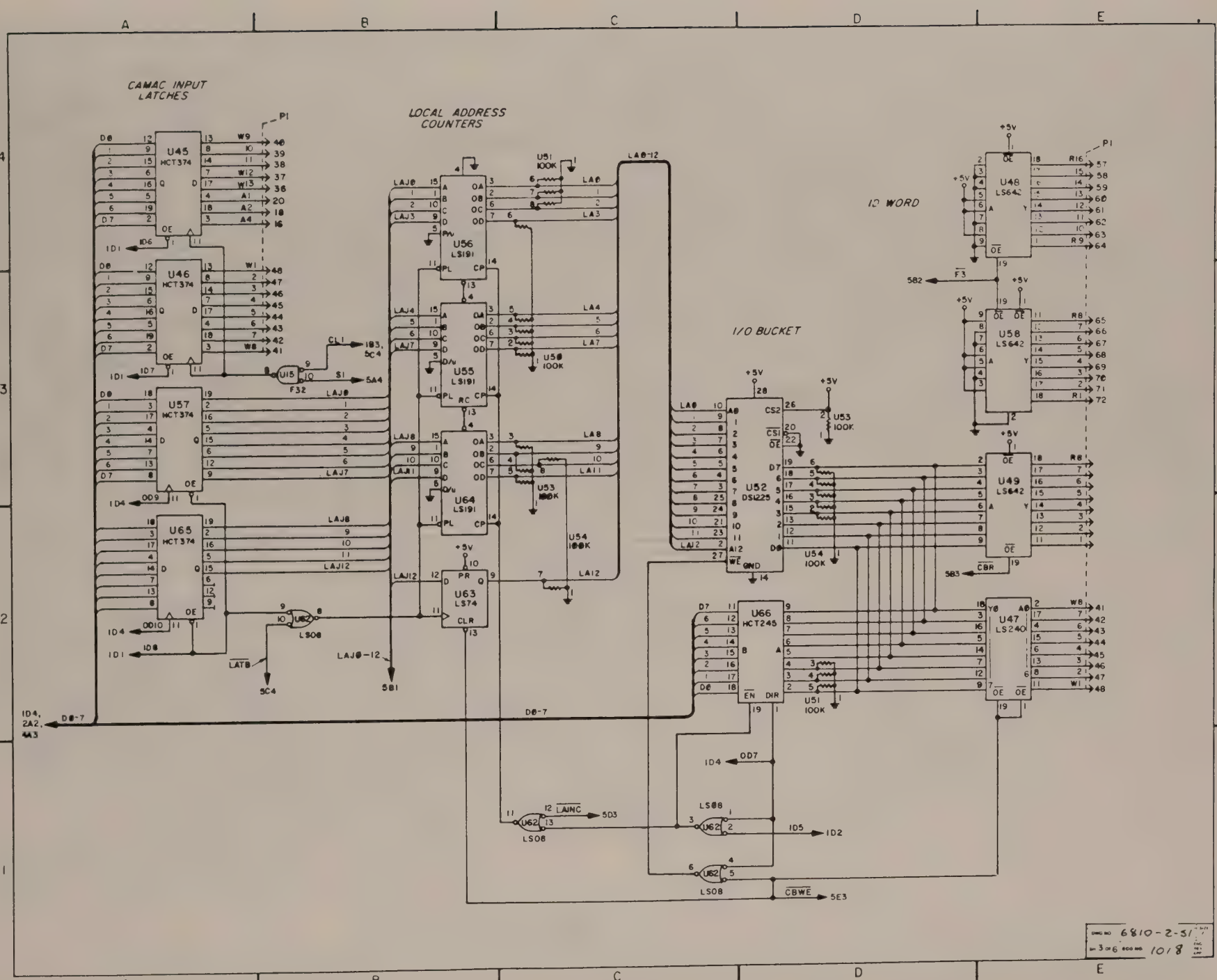
PART NUMBER	DESCRIPTION	QUANTITY PER
102412470	CAP CERA DISC 100V 47 PF	1
102484471	CAP CERA DISC 100V 470 PF	1
103317222	CAP CERA MONO 50V 2200 PF	2
103327103	CAP CERA MONO 50V .01 UF	1
103347155	CAP CERA MONO 50V 1.5 UF	2
103427104	CAP CERA MONO 100V .1 UF	71
116305100	CAP DIP MICA DM 5 10 PF	2
116515220	CAP DIP MICA DM10 22 PF	2
142824475	CAP TANT DIP CASE 4.7 UF	1
142824685	CAP TANT DIP CASE 6.8 UF	16
158849010	CAP VARIABLE 1 - 5 PF	1
161225101	RES CARBON FILM 100 OHMS	2
161225102	RES CARBON FILM 1 K	4
161225103	RES CARBON FILM 10 K	1
161225104	RES CARBON FILM 100 K	1
161225111	RES CARBON FILM 110 OHMS	1
161225121	RES CARBON FILM 120 OHMS	2
161225122	RES CARBON FILM 1.2 K	1
161225151	RES CARBON FILM 150 OHMS	1
161225202	RES CARBON FILM 2 K	8
161225271	RES CARBON FILM 270 OHMS	3
161225471	RES CARBON FILM 470 OHMS	3
161225474	RES CARBON FILM 470 K	2
161225682	RES CARBON FILM 6.8 K	1
168531303	RES PREC RN55D 115 OHMS	2
168531393	RES PREC RN55D 1.00 K	4
168531401	RES PREC RN55D 1.21 K	2
168531443	RES PREC RN55D 3.32 K	2
168531460	RES PREC RN55D 4.99 K	2
168531579	RES PREC RN55D 86.6 K	1
168531680	RES PREC RN55D 976 K	1
180247101	RES VARI CERMET 100 OHMS	1
190042222	RESISTOR NETWORK 2.2 K	2
190042472	RESISTOR NETWORK 4.7 K	1
190642104	RESISTOR NETWORK 100 K	2
190642472	RESISTOR NETWORK 4.7 K	1
190842104	RESISTOR NETWORK 100 K	2
190842472	RESISTOR NETWORK 4.7 K	1
200031028	IC 2-INPUT NAND SN74LS00N	3
200031033	IC 2-INPUT NAND SN7403N	1
200031049	IC D-TYP FLOP SN74LS74N	6
200031051	IC 2-INPUT NOR SN74LS02N	3
200031058	IC 2-INPUT AND 7409P	1
200031073	IC 2-IN POS OR SN74LS32N	3
200031077	IC 3-INPUT AND SN74LS11N	1
200031086	IC 2-INPUT AND SN74LS08N	4
200041042	IC UP/DN COUNT SN74LS191N	8
200041050	IC 4-BIT COUNT SN74LS390N	1
200041057	IC LATCH SN74LS279N	2
200071001	IC 8 X BUFFER SN74LS240	2
200071373	IC D-TYP LATCH 74LS373N	1
200071642	IC BUS TRANSCVR SN74LS642	3
200330000	IC 2-INPUT NAND 74F00	1
200330004	IC FAST HEX INV 74F04	2

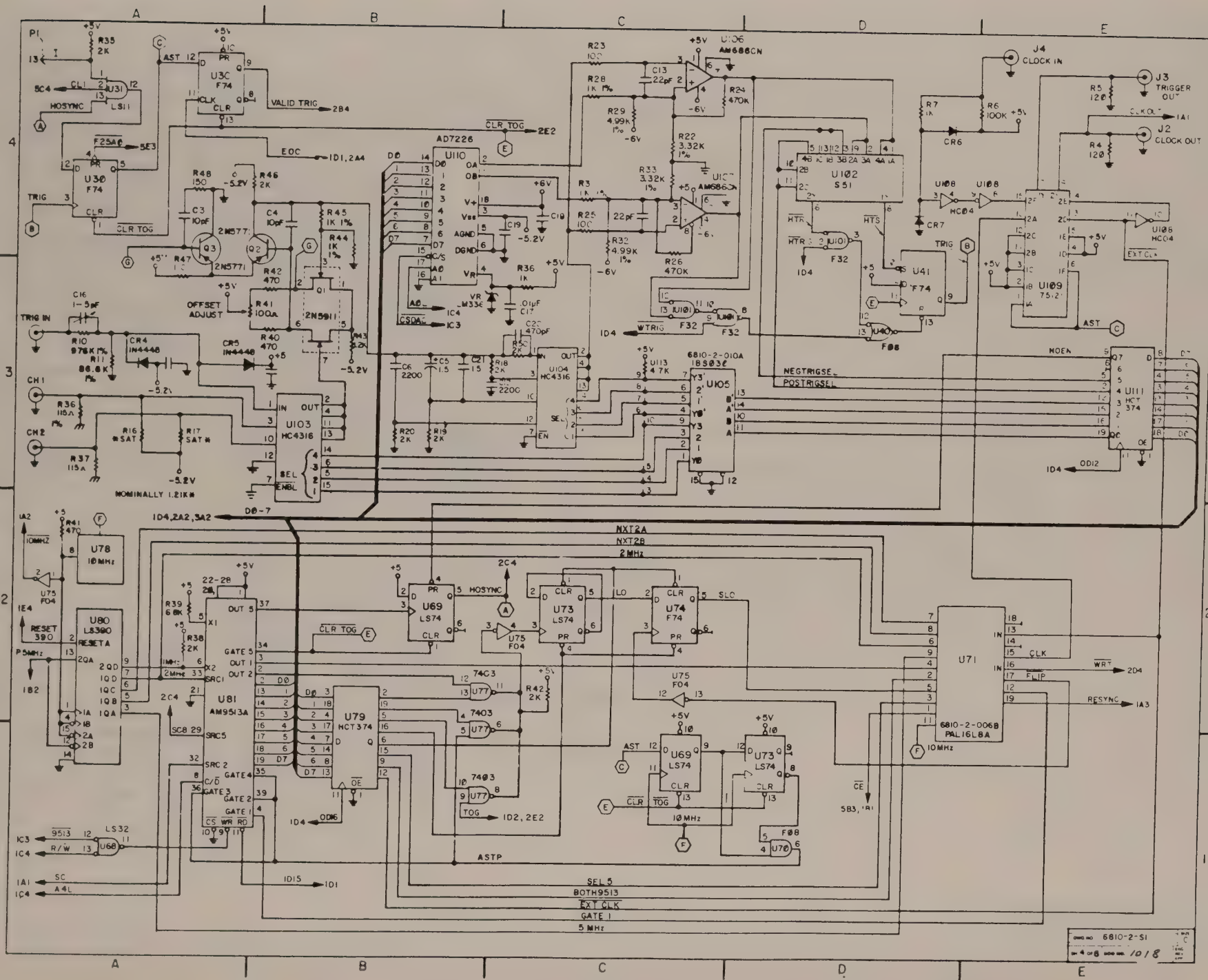
PART NUMBER	DESCRIPTION	QUANTITY PER
200330008	IC 2-INPUT AND GATE 74F08	3
200330032	IC 2-INPUT OR 74F32	2
200330051	IC AND-OR-INV GT SN74S51N	1
200331004	IC HEX INVERTER MM74HC04	1
200340074	IC D-TYPE POS FLOP 74F74	4
200373016	IC 16-IN AND-OR 16R8A	1
200373374	IC D-TYP FLOP 74HCT374	16
200380154	IC 4-TO-16 DECODR 74HC154	2
200440292	IC FREQ DIV/TIMER 74LS292	1
200440592	IC 8-BIT BINARY CTR LS592	4
200670373	IC LATCH 74F373PC	3
202246803	IC MICROCOMPUTER/MPU 6803	1
202440513	IC SYST TIMING CONTR 9513	1
205171225	IC 64K NONVOL MEMORY 1225	1
205340030	IC 32-WORD PROM 18SA030	1
205341030	IC 32X2-BIT ROM TBP18S030	1
205350349	IC 512X8-BIT PROM 74S472	3
205381732	IC 32K UV E-PROM 2732A	1
205750016	IC 16-IN AND-OR GATE 16R4	1
205750168	IC 7-WIDE AND-OR-INV 16L8	1
205782210	IC PAL 22V10	1
207140121	IC LINE DRIVER 75121	1
207277226	IC 8-BIT DAC AD7226	1
207344316	IC QUAD ANALOG SWITCH HC4316	2
207472245	IC BUS TRANSCVR HCT245	3
208517705	IC VOLTAGE REG 7705	1
208590336	IC VOLT REFERENCE LM336	1
208610686	IC VOLTAGE COMP AM686	2
230110005	DIODE SWITCHING 1N4448	4
235010005	DIODE RECTIFIER 1N4005	1
235050001	DIODE RECTIFIER 1N4139	1
256282026	DIODE RED LED	3
275170002	TRANSISTOR PNP 2N5771	2
280150911	TRANS DUAL FET "N" 2N5911	1
290180030	DELAY LINE TTL 30 N-SEC	1
300050001	CHOKE FERRITE SINGLE LEAD	2
309041010	CRYSTAL OSCILLATOR 10 MHZ	1
400061040	SOCKET IC SOLDTAIL DIP-40	2
400170020	SOCKET IC ST DIP-20	6
400341024	SOCKET IC ST DIP-24	1
402130001	CONN LEMO RT ANGLE PC MTG	1
403181002	HDR SINGL ROW STRAIGHT 2	1
403181003	HDR SINGL ROW 3	2
405764007	SOCKET SINGLE WIRE CLOSED	4
433220002	FUSE PICO II 125V 3 AMP	1
433221004	FUSE PICO II 125V 1 AMP	1
453110040	CONN FLAT CABLE MALE 40	2
454370002	SHUNT 2 POS	2
454420032	HDR SOLD TAIL/FEM 32	1
454712002	HDR SOLD TAIL/MALE 2	2
454713020	HDR SOLD TAIL/MALE 20	1
500510004	INSULATOR MICA FOR 8-PIN	1
592030040	CABLE FLAT AWG 28 40-COND	1
716810002	PC BD PREASS'Y 6810-2	1

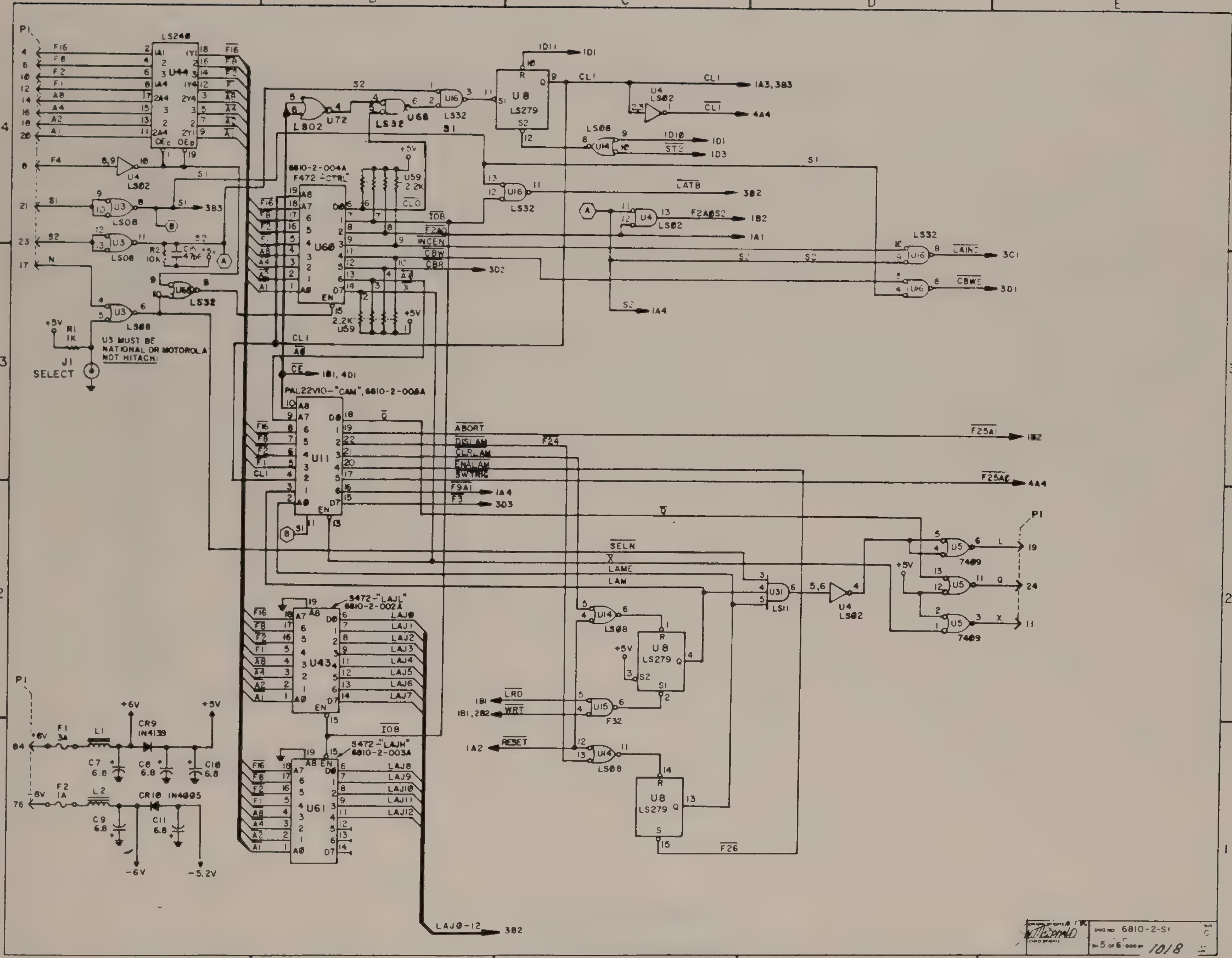
End of report. 108 Details encountered.


TRIGGERED
ARMED
READY
U38 F04
U32
U33 2.2K
U35 74HC154
U67 4.7K
U36 74HC154
U39 6116/2732A
U34 6803
U37 HCT245
U13 LS279
U27 TL7705
U9 F74
U63 LS74
U6 LS74
U29 LS00
U59 2.2K
U77 7403
U86 HCT374
U85 HCT374
U84 HCT374
U83 HCT374
U82 HCT374
U87 HCT374
U94 PI6R4
U93 LS191
U92 LS191
U91 LS191
U90 LS191
U89 LS191
U99 F373
U97 F373
U95 F373
D1 DELAY LINE SPTTLDM-30
U75 F04
U72 LS02
U70 F08
U40 F08
U69 LS32
U68 LS373
U114 4.7K
R21 270
R13 270
R8 270
R9 1K
C1 4.7
C2 0.1µF
P1
P2
P4 RAM/ROM JUMPER
P5
P6 MONITOR
LeCroy RESEARCH SYSTEMS
6810-2
6810-2-SI


STOP LATCHES
WRAP COUNTER
POST TRIGGER SAMPLE COUNTER/DIVIDER
SEQUENCER
VALID TRIG
WRT
SYNC STOP
LDWRAP
PTCENA
PTO
WRAP
CLR ACLR
ACLR
SEQPUL
MEM CLK
CE
MRST
MEMRST
NOTE:
P3 MOUNTED ON SOLDER SIDE.
6810-2-51
2 of 6
1018


CAMAC INPUT LATCHES
LOCAL ADDRESS COUNTERS
I/O BUCKET
I/O WORD
U45 HCT374
U46 HCT374
U47 LS240
U48 LS642
U49 LS642
U51 100K
U52 DS1225
U53 100K
U54 100K
U55 LS191
U56 LS191
U57 HCT374
U58 LS642
U63 LS74
U64 LS191
U65 HCT374
U66 HCT245
LS08
LAJ0-12
LA0-12
ID0-7
OD0-7
CBWE
LATB
LAINC
6810-2-51
1018


P1
U3C F74
U30 F74
U31 LS11
VALID TRIG
EOC
AD7226
U110
U106 AM686CN
U107 AM686CN
U102 S51
U41 'F74
U109 75.2'
U111 HCT 374
U105
U104 HC4316
U103 HC4316
U78 10MHz
U80 L8390 RESET A
U81 AM9513A
U79 HCT 374
U69 LS74
U73 LS74
U74 F74
U75 F04
U71 6810-2-006B PAL16L8A
U68 LS32
U70 F08
J4 CLOCK IN
J3 TRIGGER OUT
J2 CLOCK OUT
TRIG IN
OFFSET ADJUST
CH1
CH2
NOMINALLY 1.21KΩ
NEGTRIGSEL
POSTRIGSEL
NXT2A
NXT2B
2 MHz
ASTP
SEL 5
BOTH9513
EXT CLK
GATE 1
5 MHz
6810-2-51
4 of 8
10/8


LS240
U44
U4 LS02
U3 LS08
U3 MUST BE NATIONAL OR MOTOROLA NOT HITACHI
J1 SELECT
R1 1K
+5V
U16 LS32
U68 LS32
U72 LS02
U8 LS279
6810-2-004A F472 "CTRL"
U60
U59 2.2K
PAL22V10-"CAM", 6810-2-006A
U11
3472-"LAJL" 6810-2-002A
U43
3472-"LAJH" 6810-2-003A
U61
LAJ0-12
U14 LS08
U15
U31 LS11
U5 7409
ABORT
DISLAM
CLRLAM
ENALAM
SWTRIG
F9A1
F3
F24
F25A1
F25AC
F26
F32
SELN
LAME
LAM
LRD
WRT
RESET
LAINT
CBWE
LATB
CL1
WCEN
CBW
CBR
IOB
CLO
P1
L1
L2
F1 3A
F2 1A
CR9 1N4139
CR10 1N4005
C7 6.8
C8 6.8
C9 6.8
C10 6.8
C11 6.8
+6V
-6V
-5.2V
6810-2-S1
5 OF 6
1018

VOLTAGE CHART

DEVICES	REFERENCE DESIGNATION	+5V	GND	-5.2V	-6V	+8V
2.2K, SIP 8	U33, 59	1				
180K, SIP 6	U50, 53		1			
100K, SIP 8	U51, 54		1			
2732A	U39	24	12			
74HC154	U35, 36	24	12			
74F373	U95, 97, 99	20	10			
74LS240	U44, 47	20	10			
74HCT245	U37, U66, U112	20	10			
74LS373	U10	20	10			
74HCT374	U26, 45, 46, 57, 65, 79, 82, 83, 84, 85, 86, 87, 96, 98, 100, 111	20	10			
74LS642	U48, 49, 58	20	10			
P16R4	U94	20	10			
PAL16R8A	U17	20	10			
DS1225	U52	28	14			
AD7226	U110		5,6	3		18
1853A030	U32	16	8			
1850S30	U105	16	8			
74LS191	U55, 56, 64, 89, 90, 91, 92, 93	16	8			
74LS279	U8, 13	16	8			
74LS292	U21	16	8			
74LS390	U80	16	8			
74LS592	U22, 23, 24, 25	16	8			
75121	U109	16	8			
6803	U34	21,7	1			
10MHz TTL OSCILLATOR	U78	14	7			
7403	U77	14	7			
7409	U5	14	7			
74F04	U38, 75	14	7			
74F08	U2, U40	14	7			
74F74	U74, U41, U30, U9	14	7			
74HC04	U108	14	7			
74HC4316	U103, 104	16	8			
74L800	U12, 29, 42	14	7			
74LS02	U4, 7, 72	14	7			
74F32	U15, U101					
74LS08	U3, 14, 20, 62, 70	14	7			
74F00	U1					
74LS11	U31	14	7			
74LS32	U16, 19, 88	14	7			
74881	U76, 102	14	7			
74LS74	U6, 18, 28, 63, 69, 73	14	7			
TL7705	U27	8	4			
AM686	U106, 107	1	6		4	
AM9513A	U81	1	21			
AMPAL22V10	U11,	24	12			
74F472	U43, 60, 61	20	10			
PAL16L8AL	U71	20	10			

VOLTAGE CHART (CON'T)

DEVICES	REFERENCE DESIGNATION	+5V	GND	-5.2V	-6V	+8V
4.7K, SIP 10	U113	1				
4.7K, SIP 8	U67	1				
4.7K, SIP 6	U114	1				

NOTE:
1. ALL UNMARKED CAPACITORS ARE 0.1μF.
2. SOME BYPASS CAPACITORS ARE NOT ASSIGNED REFERENCE NUMBERS.

LAST REFERENCE DESIGNATION USED

U	R	CR	VR	Q	J	L	P	C	F
119	142	9	1	1	3	2	7	19	2

NOTE UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

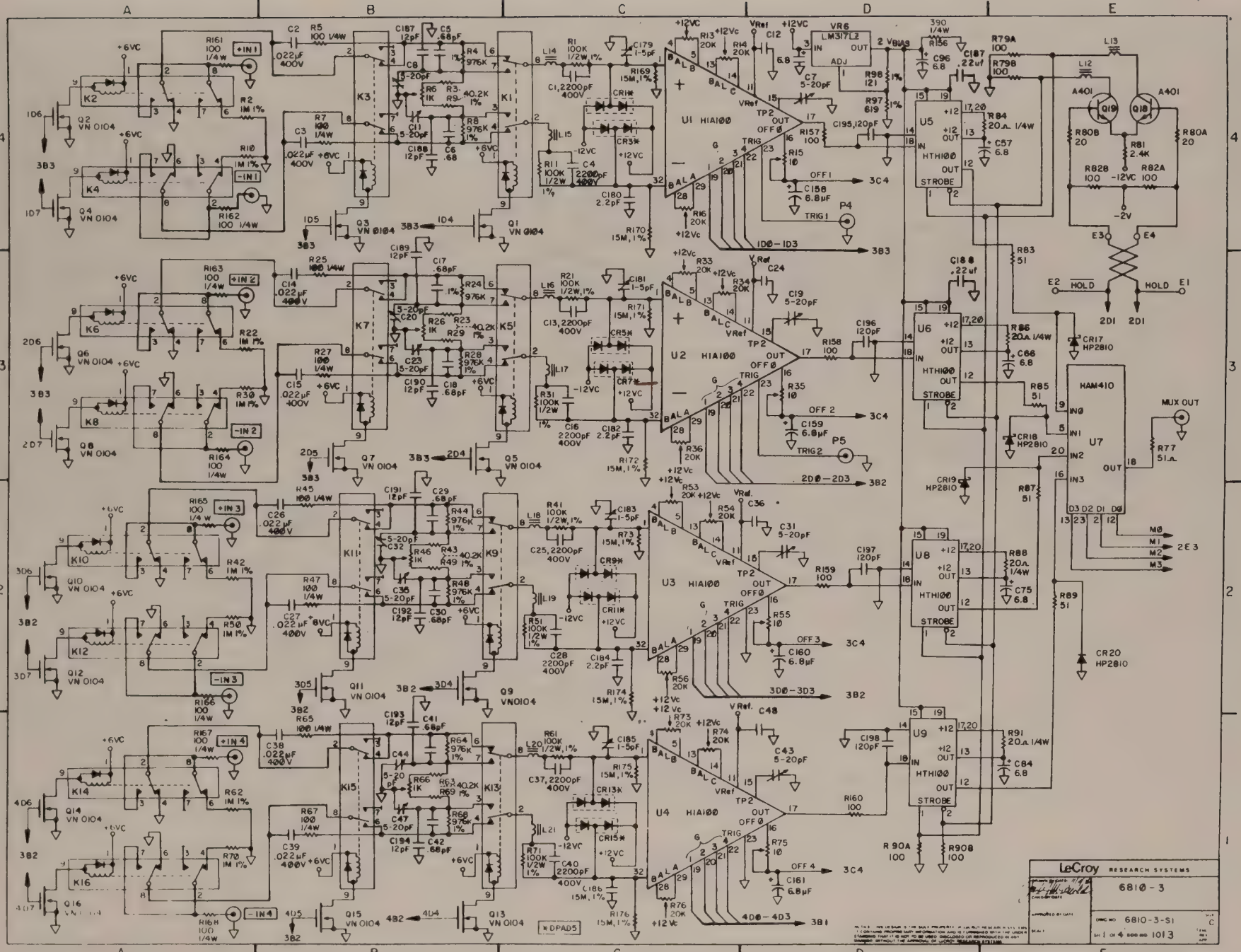
DWG NO 6810-2-S1 C
SH 6 OF 6 DOC NO 1018

PART NUMBER	DESCRIPTION	QUANTITY PER
102412022	CAP CERA DISC 100V 2.2 PF	4
102412120	CAP CERA DISC 100V 12 PF	8
102412121	CAP CERA DISC 100V 120 PF	4
102490068	CAP CERA DISC 100V .68 PF	8
103327103	CAP CERA MONO 50V .01 UF	76
103336224	CAP CERA MONO 50V .22UF	2
116515131	CAP DIP MICA DM10 130 PF	1
116515331	CAP DIP MICA DM10 330 PF	1
116515390	CAP DIP MICA DM10 39 PF	1
124775222	CAPACITOR WRAP&FILL 2200 PF	8
124775223	CAPACITOR WRAP&FILL .022UF	8
142124476	CAP TANT DIP CASE 47 UF	7
142824684	CAP TANT DIP CASE .68 UF	8
142824685	CAP TANT DIP CASE 6.8 UF	50
158899004	CAP VARIABLE 1 - 5 PF	4
158899005	CAP VARIABLE 5 - 20 PF	12
161225101	RES CARBON FILM 100 OHMS	33
161225102	RES CARBON FILM 1 K	7
161225103	RES CARBON FILM 10 K	2
161225200	RES CARBON FILM 20 OHMS	2
161225242	RES CARBON FILM 2.4 K	1
161225432	RES CARBON FILM 4.3 K	1
161225470	RES CARBON FILM 47 OHMS	2
161225471	RES CARBON FILM 470 OHMS	1
161225510	RES CARBON FILM 51 OHMS	5
161335101	RES CARBON FILM 100 OHMS	18
161335103	RES CARBON FILM 10 K	1
161335200	RES CARBON FILM 20 OHMS	4
161335391	RES CARBON FILM 390 OHMS	1
168008015	RES PREC 1% 15 MEG	8
168409392	RES RN55C .1% 976 K	8
168409549	RES RN55C .1% 40.2 K	8
168531265	RES PREC RN55D 46.4 OHMS	2
168531285	RES PREC RN55D 75.0 OHMS	1
168531305	RES PREC RN55D 121 OHMS	4
168531373	RES PREC RN55D 619 OHMS	1
168531393	RES PREC RN55D 1.00 K	2
168531397	RES PREC RN55D 1.10 K	1
168531458	RES PREC RN55D 4.75 K	1
168531493	RES PREC RN55D 11.0 K	1
168531495	RES PREC RN55D 11.5 K	1
168531681	RES PREC RN55D 1.00 MEG	8
168651585	RES PREC RN60D 100 K	8
175765043	RES PWR WW 5% 4.3 OHMS	4
180247100	RES VARI CERMET 10 OHMS	4
180247102	RES VARI CERMET 1 K	4
180247203	RES VARI CERMET 20 K	12
180247501	RES VARI CERMET 500 OHMS	1
190042562	RESISTOR NETWORK 5.6 K	1
190642101	RESISTOR NETWORK 100 OHMS	1
190642471	RESISTOR NETWORK 470 OHMS	1
190842102	RES NETWORK 1 K	1
190842471	RESISTOR NETWORK 470 OHMS	1
190842562	RESISTOR NETWORK 5.6 K	1

PART NUMBER	DESCRIPTION	QUANTITY PER
200041186	IC D-TYP FLOP F10186PC	1
200341139	IC 2-TO-4 LINE DEC HC139	1
200343174	IC HEX D-FLOP 74HC174	1
200370374	IC OCTAL FLOP 74HC374	4
200444016	IC BINARY COUNTER 10H016	1
204042002	IC NOR GATE MC10102P	1
204042004	IC 2-3-2-IN GATE MC10105P	1
204042005	IC TYP D FL-FL MC10131P	1
204042008	IC QUAD TRANSL MC10125P	1
204042012	IC 2-IN AND GATE MC10104P	3
204042015	IC LINE RECEIVER MC10114P	1
204042103	IC 2-IN OR GATE MC10103P	1
204042162	IC 1-OF-8 DECODER F10162P	1
207277226	IC 8-BIT DAC AD7226	1
208011011	IC JFET OP AMP TL082CP	2
208031010	IC QUAD DIFF COMP LM339N	1
208111056	IC OP AMP JFET 1056	3
208122337	IC ADJ -VOLT REG LM337T	2
208211002	IC VOLT REF REF-02DP	1
208510317	IC ADJ +V REG 317LZ	1
208570317	IC ADJ +V REG LM317	1
230040005	DIODE DUAL PICO-AMP DPAD5	8
230110005	DIODE SWITCHING 1N4448	3
240225716	DIODE ZENER 12V 1N5242	1
240345929	DIODE ZENER 15V 1N5929A	2
240423958	DIODE ZENER 7.5V 1N958B	1
253010810	DIODE HOT CARRIER HP2810	4
270110003	TRANSISTOR NPN 2N2222A	1
270130401	TRANSISTOR NPN A401	2
280170104	TRANSISTOR FET N VN0104N3	16
280190531	TRANSISTOR "N" CH IRF531	2
290140500	DELAY LINE 500 N-SEC	1
290141125	DELAY LINE 125 NS	2
300010001	BEAD SHIELDING FERRITE	12
300050001	CHOKE FERRITE SINGLE LEAD	10
399011016	SOCKET SOLDER TAIL SIP-16	8
402020000	CONNECTOR CO-AXIAL BNC	4
402020001	GROUND LUG NONLOCKING BNC	4
402080000	CONNECTOR BNC ISOLATD GND	8
402611001	CONN CO-AX CABLE END SMB	1
403181002	HDR SINGL ROW STRAIGHT 2	1
405120002	CONN HOUSING 2-POS	2
405734012	CONTACT CRIMPED WIRE END	12
405764007	SOCKET SINGLE WIRE CLOSED	8
430640001	RELAY 2 FORM C DPDT	16
433220002	FUSE PICO II 125V 3 AMP	2
433222005	FUSE PICO II 125V 2 AMP	2
454420032	HDR SOLD TAIL/FEM 32	5
471111001	BUS BAR 1-CONDUCTOR	3
471161001	BUS BAR 1-CONDUCTOR	3
500110001	TRANSIPAD "SMALL"	10
500120003	MOUNTING PAD 10-LEAD RED	16
500860302	INSULATOR FOR TO-220	5
505070002	HEAT SINK FOR TO-220	5

PART NUMBER	DESCRIPTION	QUANTITY PER
567440006	SCREW FLAT PHIL 4-40X3/8	2
574409005	WASHER SHOULDER NYLON #4	5
591692330	WIRE TEFLON TW PR AWG 30	0
593910001	CABLE CO-AXIAL RG178B/U	2
593920002	CABLE CO-AXIAL RG 188 A/U	1
716810003	PC BD PREASS'Y 6810-3	1
HAM410	HYBRID AMPL MULTIPLEX	1
HIA100	HYB INSTR AMPL HIA100	4
HTH100	HYB TRACK & HOLD	4

End of report. 117 Details encountered.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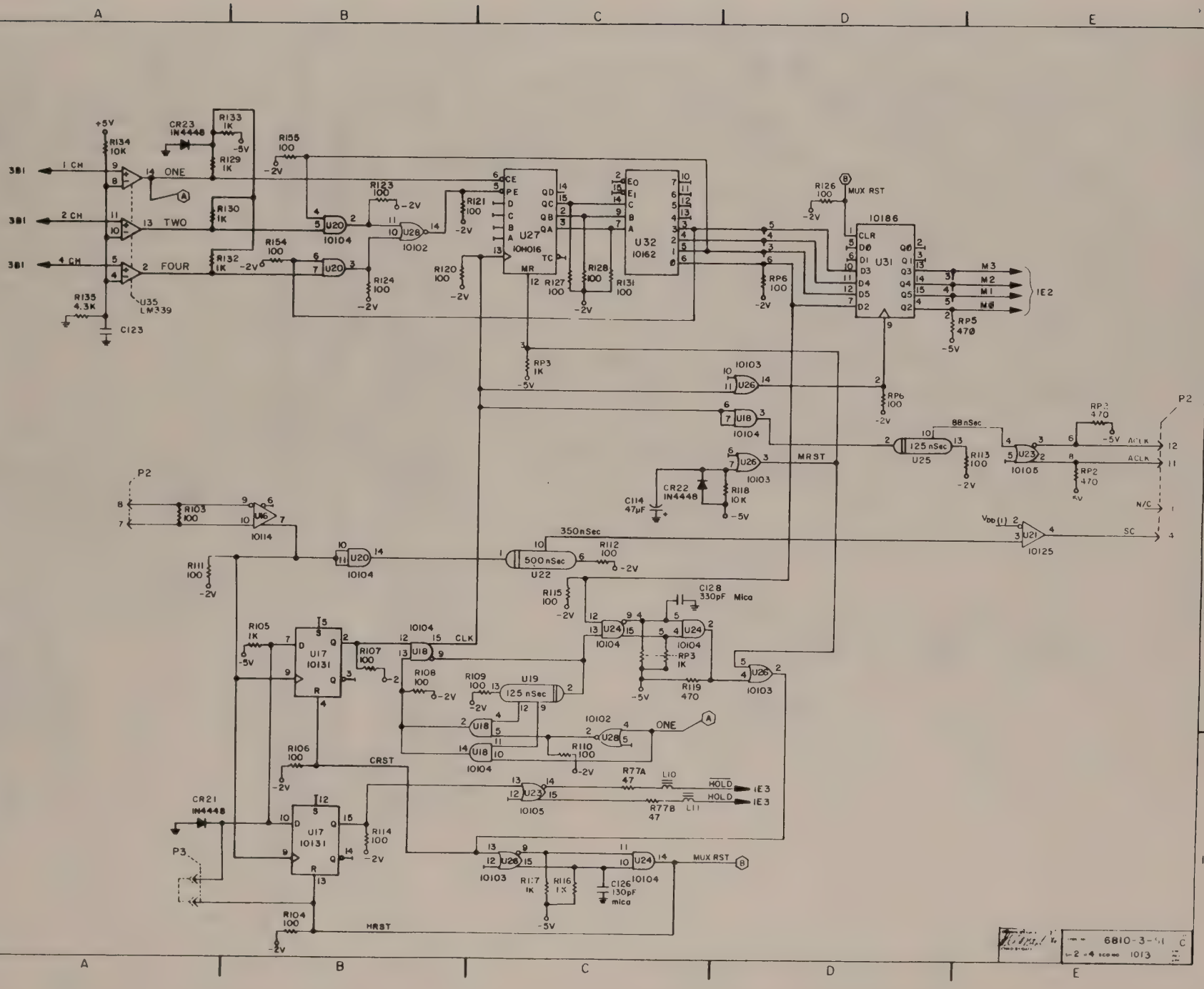
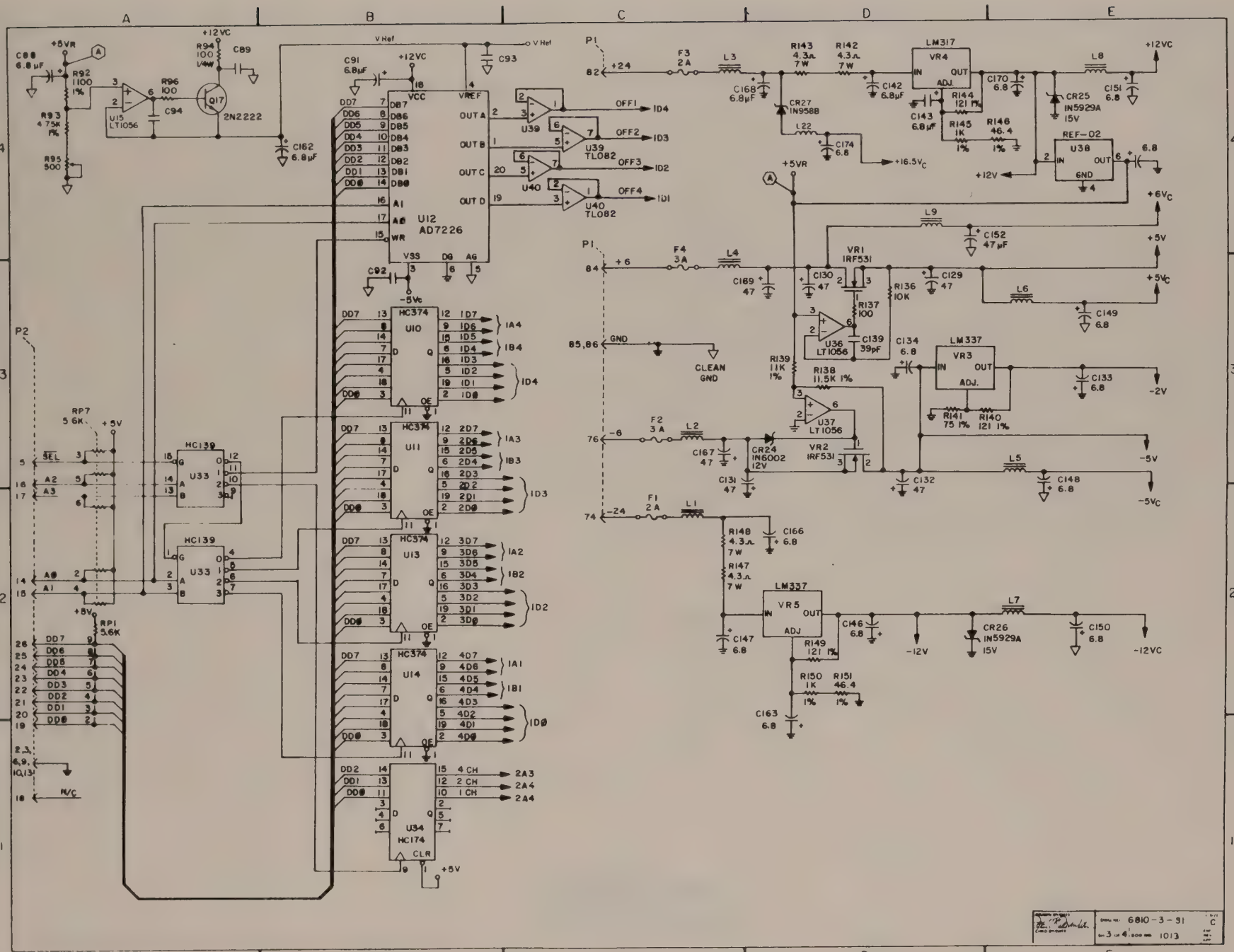
+IN2
+IN3
+IN4
-IN1
-IN2
-IN3
-IN4
U1 HIA100
U2 HIA100
U3 HIA100
U4 HIA100
LM317L2
HTHI00
HAM410
U5
U6
U7
U8
U9
Q19
Q18
A401
LeCroy RESEARCH SYSTEMS
6810-3
6810-3-S1
MUX OUT
HOLD
TRIG1
TRIG2
OFF 1
OFF 2
OFF 3
OFF 4
3C4
3B2
3B3
2D1
2E3
3B1
4D3
*DPAD5


381 1 CH
381 2 CH
381 4 CH
ONE
TWO
FOUR
U35 LM339
+5V
-5V
-2V
U27 10H016
U32 10162
10186
U31
M3
M2
M1
M0
IE2
MUX RST
MRST
HRST
CRST
CLK
U17 10131
U19 125 nSec
U22 500 nSec
U25 125 nSec
88nSec
350nSec
U21 10125
C128 330pF Mica
C114 47µF
C123
C126 130pF mica
CR21 IN4448
CR22 IN4448
CR23 IN4448
HOLD
IE3
ACLK
SC
N/C
P2
P3


+5VR
+12VC
-5Vc
V Ref
U12
AD7226
VCC
VREF
OUT A
OUT B
OUT C
OUT D
VSS
DG
AG
U39
TL082
U40
TL082
OFF1
OFF2
OFF3
OFF4
ID4
ID3
ID2
ID1
U10
U11
U13
U14
HC374
HC139
U33
U34
HC174
RP1
5.6K
RP7
5.6K
P1
P2
+24
+6
-6
-24
GND
CLEAN GND
F1 2A
F2 3A
F3 2A
F4 3A
LM317
VR4
LM337
VR5
VR3
VR1 IRF531
VR2 IRF531
U36 LT1056
U37 LT1056
REF-02
U38
+16.5Vc
+6Vc
+5Vc
-2V
-5V
-5Vc
-12V
-12VC
CR24 IN6002 12V
CR25 IN5929A 15V
CR26 IN5929A 15V
CR27 IN9588
2N2222
Q17
U15 LT1056
6810-3-91
C
1013

DEVICE	REFERENCE DESIGNATION	+16.5VC	+12V	+12VC	+5VC	+5V	-5V	-5VC	-12VC	-12V	AGND	GND
HIA100	U1, 2, 3, 4	18		10					24		2, 9 12, 31	
HTH100	U5, 6, 8, 9			17, 20	22			6, 10	4, 8		3, 7, 11, 14, 16, 21 24	
10H016	U27						8					1, 16
10102	U28						8					1, 16
10103	U26						8					1, 16
10104	U18, 20, 24						8					1, 16
10105	U23						8					1, 16
10114	U16						8					1, 16
10125	U21					9	8					16
10131	U17						8					1, 16
10162	U32						8					1, 16
10186	U31						8					16
AD7226	U12			18				3			5	6
LT1086	U15			7					4			
LT1056	U36, 37		7							4		
LM339	U35					3	12					
74HC374	U10, 11, 13, 14					20						10
74HC139	U33					14						7
74HC174	U34					16						8
500nSec	U22											7, 14
125nSec	U19, 25											1, 14
HAM410	U7			3				14	22		1, 4, 6, 7, 8, 10, 15 17, 19, 21, 24	
REF02	U38		2									4
TL082	U39, 40			8					4			
UNUSED	U29, 30											

UNUSED DEVICES:

10102	U28	6, 7, 3; 12, 13, 15; 9
10104	U20	12, 13, 15, 9
10105	U23	9, 10, 11, 6, 7
10125	U21	6, 7, 5; 10, 11, 12; 14, 15, 13
LM339	U35	7, 6, 1
10104	U24	6, 7, 3
10114	U16	12, 13, 14, 15, 4, 5, 2, 3

UNMARKED CAPS ARE .01 μF.

LAST REFERENCE DESIGNATION USED

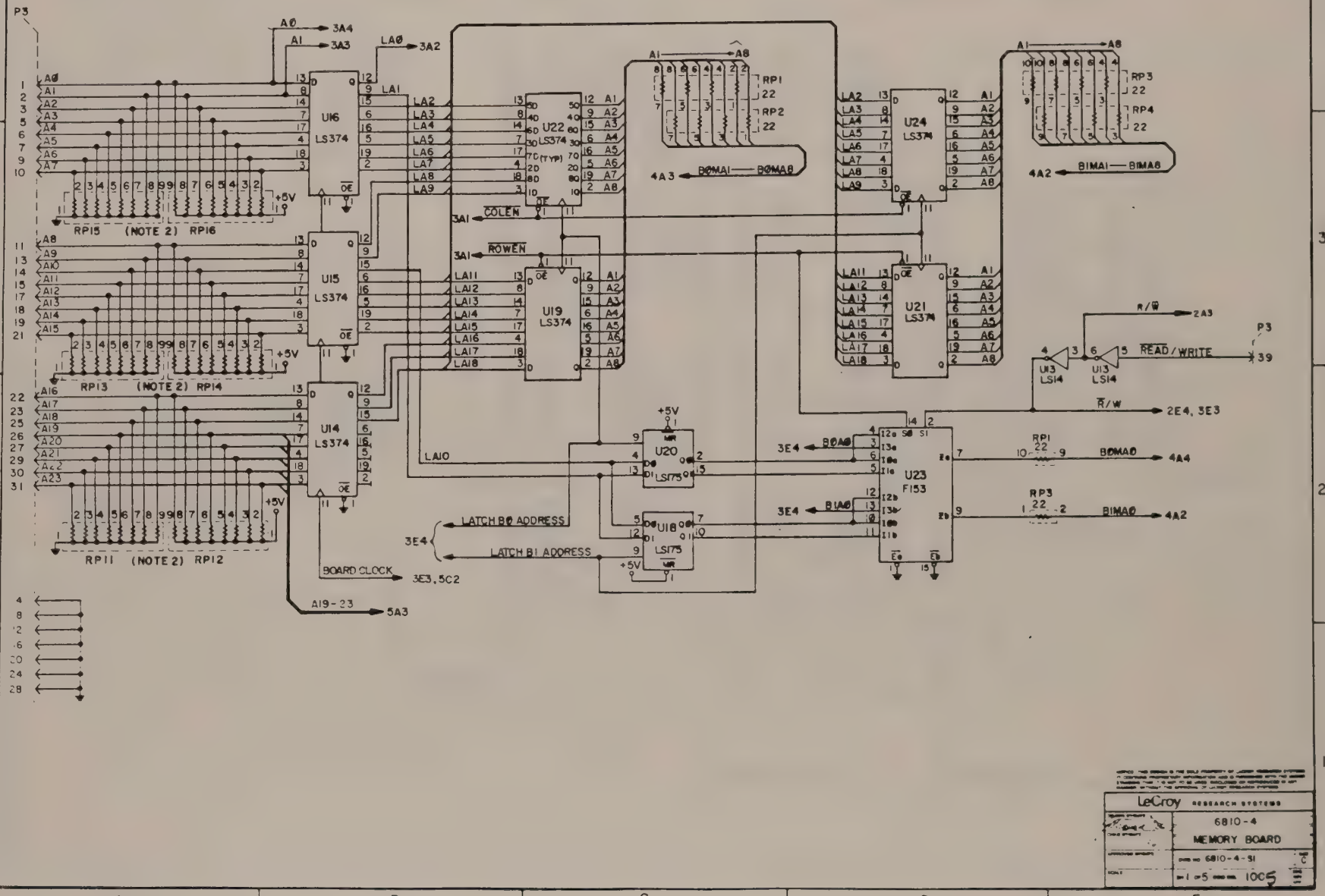
U	CN	CR	Q	C	S	P	F	L		VR	R	RP	K
40	4	27	19	108	4	5	4	22		6	156	7	16

NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

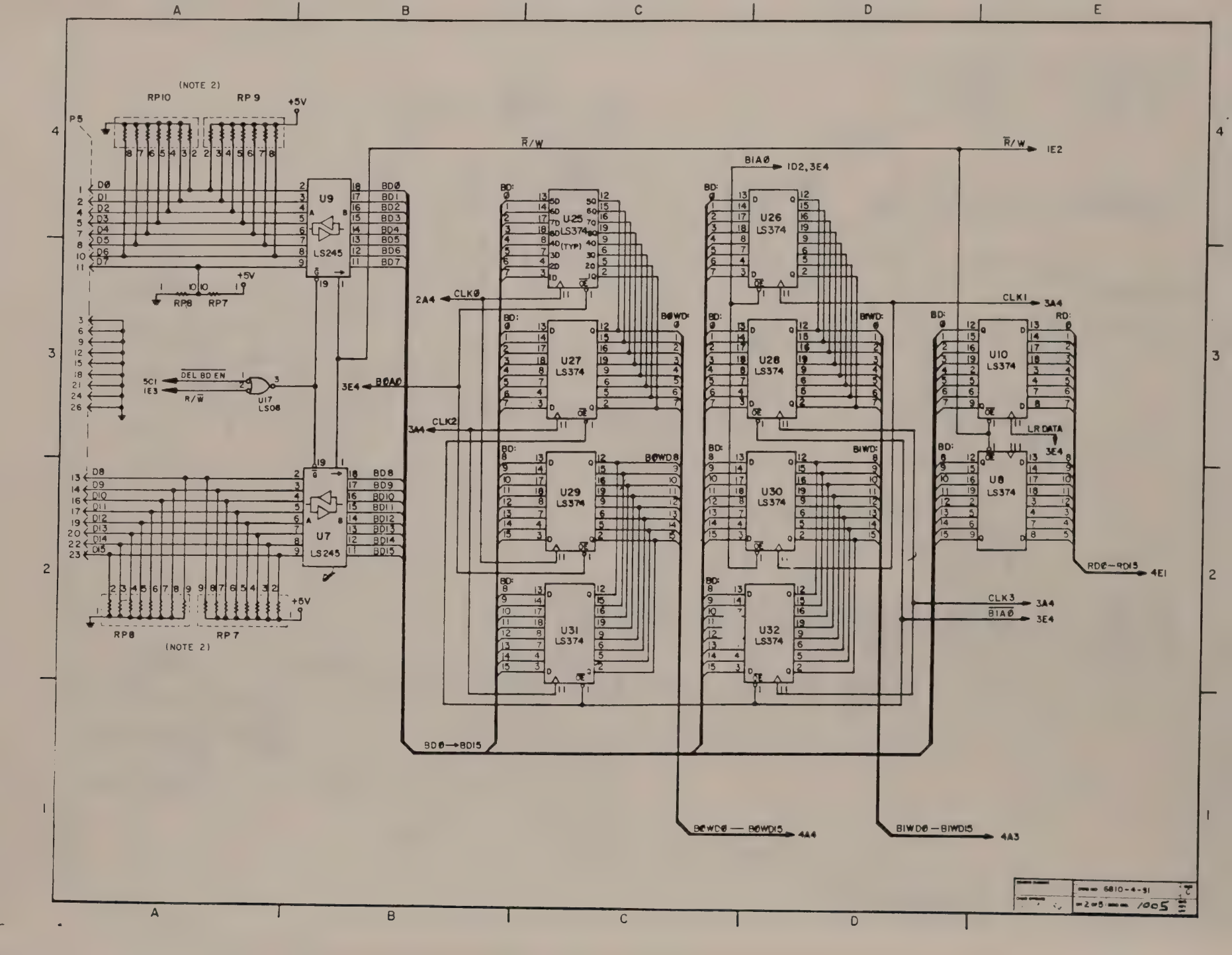
DWG NO 6810-3-51 REV C
SHT 4 OF 4 SIZE D 1013

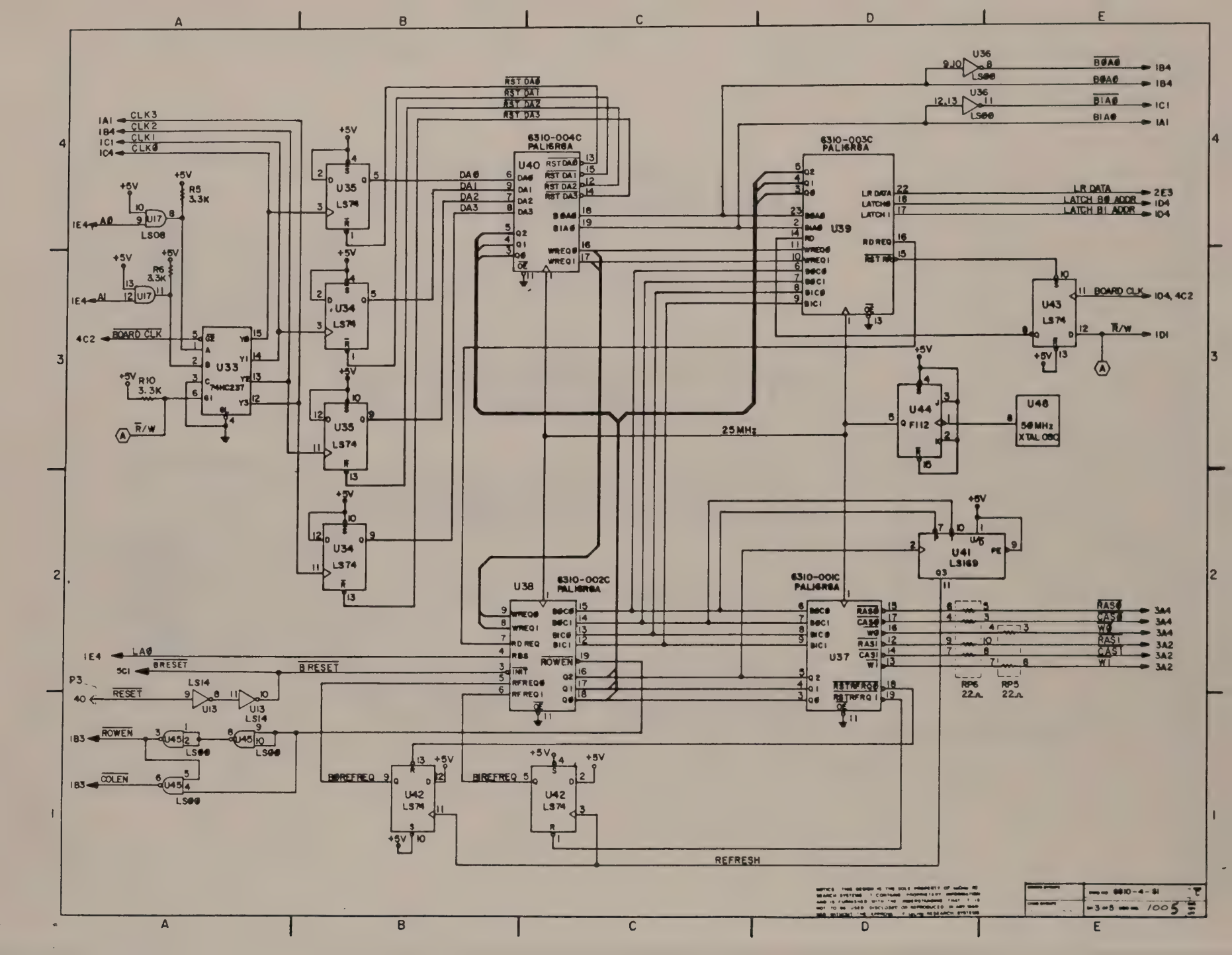
PART NUMBER	DESCRIPTION	QUANTITY PER
102090303	CAP IC DECOUPLING DIP-16	5
102092303	CAP IC DECOUPLING DIP-20	4
103276104	CAP CERA MONO X7R .1 UF	32
103427104	CAP CERA MONO 100V .1 UF	21
142824685	CAP TANT DIP CASE 6.8 UF	13
161225102	RES CARBON FILM 1 K	2
161225103	RES CARBON FILM 10 K	2
161225332	RES COMP 1/8W 5% 3.3 K	3
190052220	RESISTOR NETWORK 22 OHMS	6
200031049	IC D-TYP FLOP SN74LS74N	4
200031073	IC 2-IN POS OR SN74LS32N	1
200031086	IC 2-INPUT AND SN74LS08N	1
200031095	IC HEX INVERTER SN74LS14N	1
200041049	IC D-TYP FLOP SN74LS175N	2
200041065	IC UP/DN CNTR SN74LS169AN	1
200041071	IC FULL ADDER SN74LS283N	4
200071003	IC 8-BIT REGIST SN74LS374	13
200071007	IC BUFFER SN74LS244N	1
200071245	IC BUS XCEIVER SN74LS245N	2
200331000	IC QUAD 2-IN NAND 74LS00	2
200340112	IC J-K NEG FLOP 74F112	1
200340237	IC 3-TO-8 DECODER 74HC237	1
200371374	IC D-TYP FLOP 74F374PC	4
200373016	IC 16-IN AND-OR 16R8A	3
200380108	IC 20-IN AND-OR 20R8A	1
200570685	IC 8BIT MAGN COMP 74LS685	2
205240256	IC RAM HM50256-15	24
207340153	IC 4-IN MULTIPLEXR 74F153	1
235050001	DIODE RECTIFIER 1N4139	1
300050001	CHOKE FERRITE SINGLE LEAD	1
309040050	CRYSTAL OSCILLATOR 50 MHZ	1
400041024	SOCKT IC SOLD TAIL DIP-24	1
400071020	SOCKET IC ST DIP-20	3
403181002	HDR SINGL ROW STRAIGHT 2	2
403181003	HDR SINGL ROW 3	1
405812002	SOCKET STRIP SOLDR 20 POS	1
433225001	FUSE PICO II 125V 5 AMP	1
454370002	SHUNT 2 POS	1
454420032	HDR SOLD TAIL/FEM 32	3
485021002	BUMPER TAPERED SQUARE	1
591664030	WIRE BLU SOLID AWG 30	1
706810041	STIFFENER PC BOARD	1
716310000	PC BD PREASS'Y 6310	1

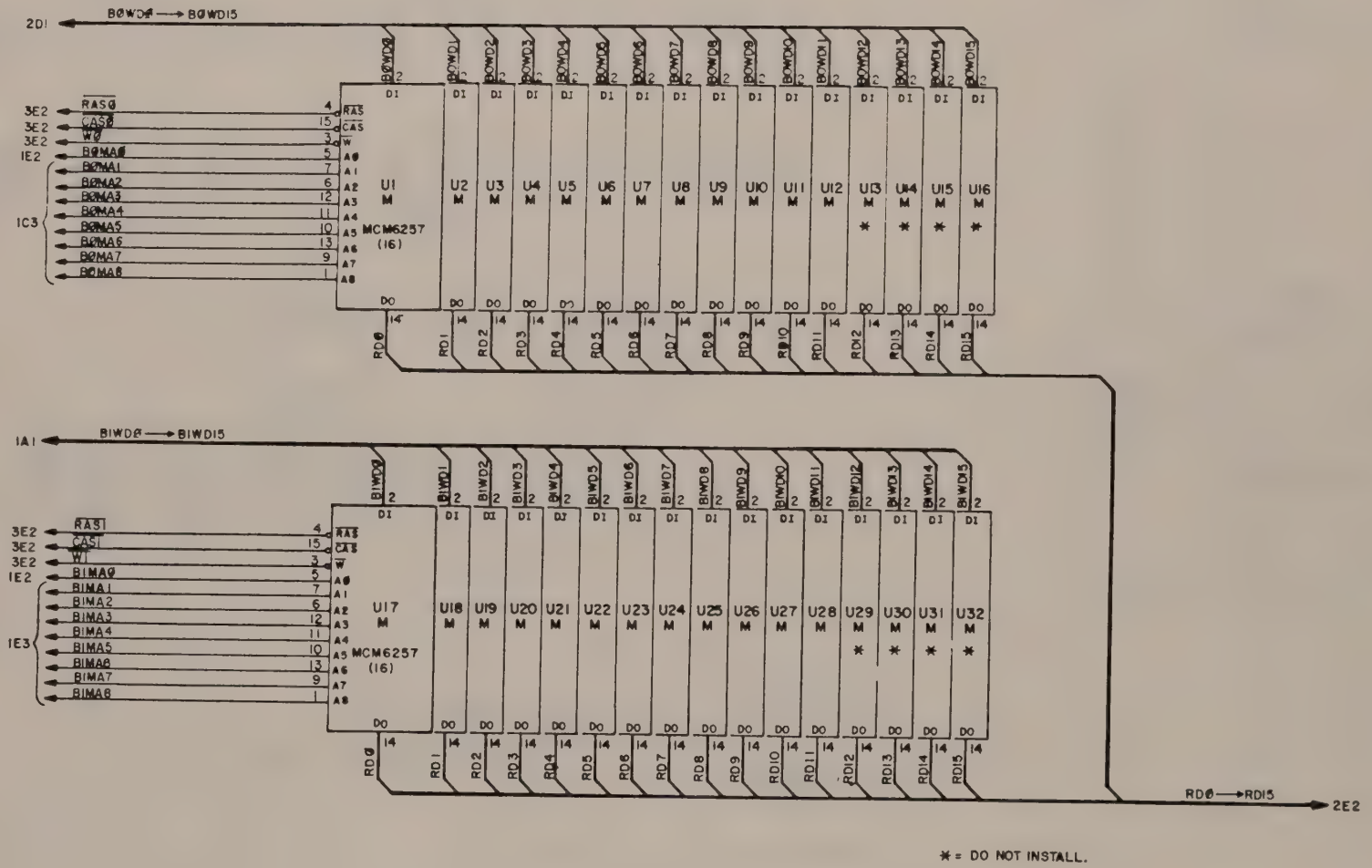
End of report. 43 Details encountered.

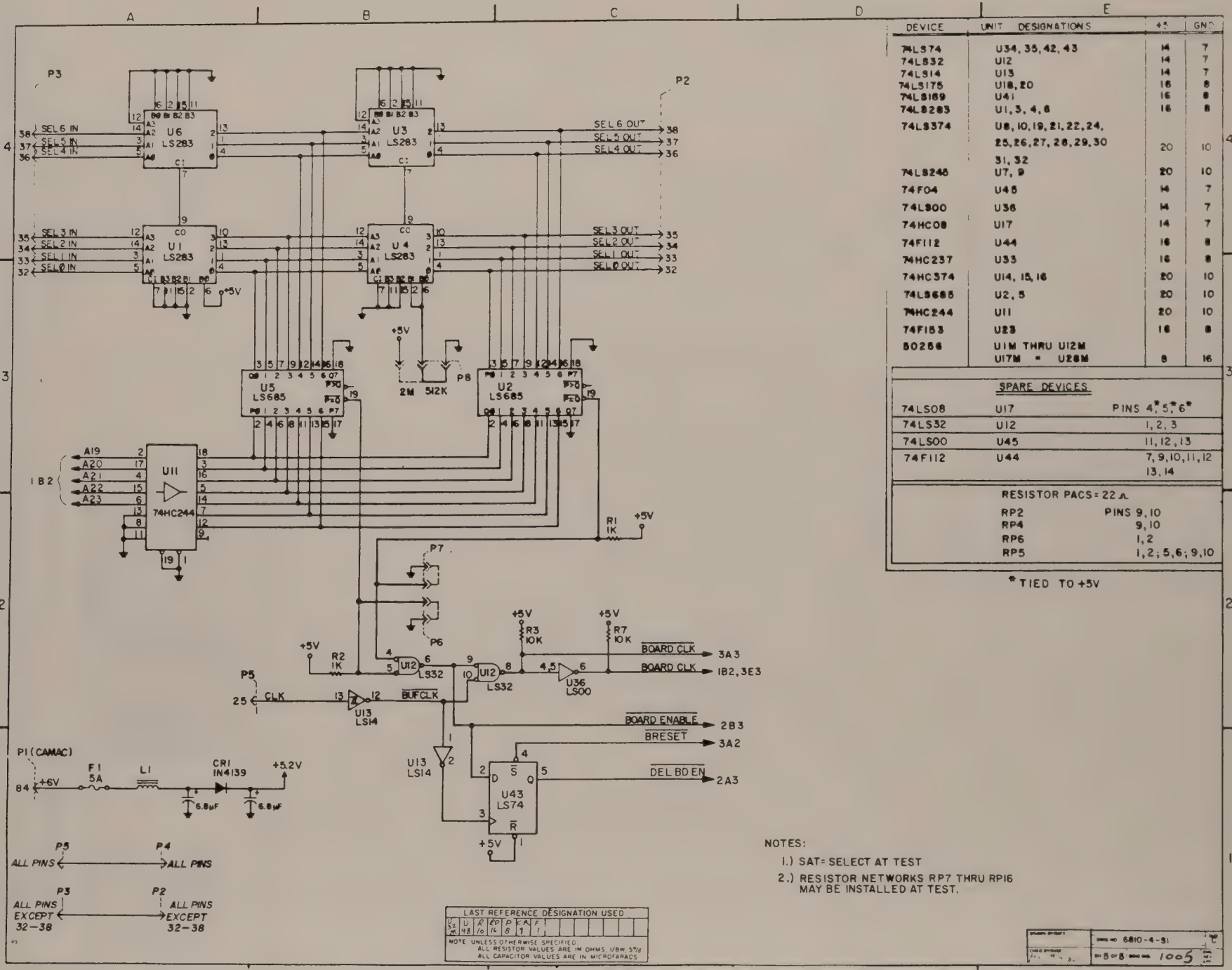


LeCroy RESEARCH SYSTEMS	
	6810-4
	MEMORY BOARD
	6810-4-SI
	1 OF 5 1005


(NOTE 2)
RP10
RP9
+5V
P5
D0
D1
D2
D3
D4
D5
D6
D7
U9
LS245
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
RP8
RP7
R/W
DEL BD EN
5C1
1E3
U17
LS08
3E4
B0A0
D8
D9
D10
D11
D12
D13
D14
D15
U7
LS245
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
(NOTE 2)
CLK0
2A4
CLK2
3A4
U25
LS374
(TYP)
U27
LS374
U29
LS374
U31
LS374
B0WD:
B0WD8
BD0→BD15
B1A0
1D2,3E4
U26
LS374
U28
LS374
U30
LS374
U32
LS374
B1WD:
CLK1
CLK3
U10
LS374
U8
LS374
LRDATA
RD:
RD0—RD15
4E1
B0WD0 — B0WD15
4A4
B1WD0—B1WD15
4A3
1E2


U40
6310-004C
PAL16R8A
U39
6310-003C
PAL16R8A
U38
6310-002C
PAL16R8A
U37
6310-001C
PAL16R8A
U35
LS374
U34
LS374
U33
74HC237
U43
LS74
U44
F112
U41
LS169
U42
LS74
U45
LS08
U36
LS00
U17
LS08
U13
LS14
U46
56MHz
XTAL OSC
RP6
22Ω
RP5
22Ω
R5
3.3K
R6
3.3K
R10
3.3K
CLK3
CLK2
CLK1
CLK0
BOARD CLK
R/W
25MHz
REFRESH
ROWEN
COLEN
BRESET
RESET
LA0
RST DA0
RST DA1
RST DA2
RST DA3
DA0
DA1
DA2
DA3
LR DATA
LATCH B0 ADDR
LATCH B1 ADDR
RAS0
CAS0
WE0
RAS1
CAS1
WE1


2D1
B0WD0 → B0WD15
3E2 RAS0
3E2 CAS0
3E2 W0
1E2 B0MA0
B0MA1
B0MA2
B0MA3
B0MA4
1C3 B0MA5
B0MA6
B0MA7
B0MA8
U1 M
U2 M
U3 M
U4 M
U5 M
U6 M
U7 M
U8 M
U9 M
U10 M
U11 M
U12 M
U13 M *
U14 M *
U15 M *
U16 M *
MCM6257 (16)
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
RD12
RD13
RD14
RD15
1A1
B1WD0 → B1WD15
3E2 RAS1
3E2 CAS1
3E2 W1
1E2 B1MA0
B1MA1
B1MA2
B1MA3
B1MA4
1E3 B1MA5
B1MA6
B1MA7
B1MA8
U17 M
U18 M
U19 M
U20 M
U21 M
U22 M
U23 M
U24 M
U25 M
U26 M
U27 M
U28 M
U29 M *
U30 M *
U31 M *
U32 M *
MCM6257 (16)
RD0 → RD15
2E2
* = DO NOT INSTALL.



DEVICE	UNIT DESIGNATIONS	+5	GND
74LS74	U34, 35, 42, 43	14	7
74L832	U12	14	7
74LS14	U13	14	7
74LS175	U18, 20	16	8
74LS169	U41	16	8
74LS283	U1, 3, 4, 6	16	8
74LS374	U8, 10, 19, 21, 22, 24, 25, 26, 27, 28, 29, 30 31, 32	20	10
74LS245	U7, 9	20	10
74F04	U45	14	7
74L800	U36	14	7
74HC08	U17	14	7
74F112	U44	16	8
74HC237	U33	16	8
74HC374	U14, 15, 16	20	10
74LS685	U2, 5	20	10
74HC244	U11	20	10
74F153	U23	16	8
80256	U1M THRU U12M U17M = U28M	8	16

SPARE DEVICES

74LS08	U17	PINS 4*, 5*, 6*
74LS32	U12	1, 2, 3
74LS00	U45	11, 12, 13
74F112	U44	7, 9, 10, 11, 12 13, 14

RESISTOR PACS = 22Ω

RP2	PINS 9, 10
RP4	9, 10
RP6	1, 2
RP5	1, 2; 5, 6; 9, 10

*TIED TO +5V

NOTES:

1.) SAT= SELECT AT TEST

2.) RESISTOR NETWORKS RP7 THRU RP16 MAY BE INSTALLED AT TEST.

LAST REFERENCE DESIGNATION USED

U	U	R	RP	P	E	A	F
32	48	10	16	8	9	1	

NOTE UNLESS OTHERWISE SPECIFIED:
ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

DWG NO 6810-4-81

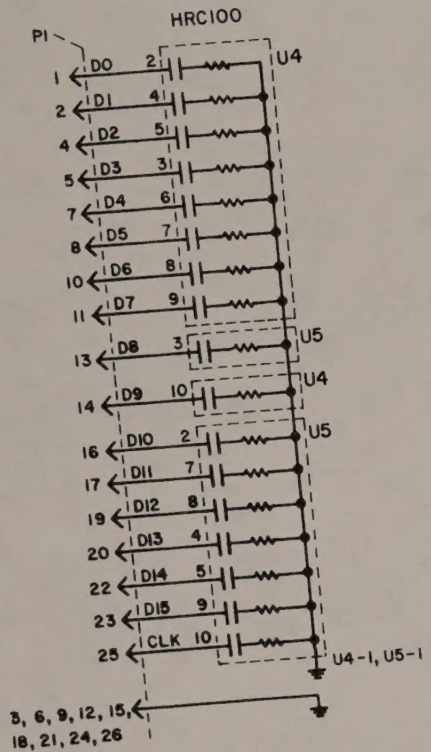
SH 5 OF 8

1005

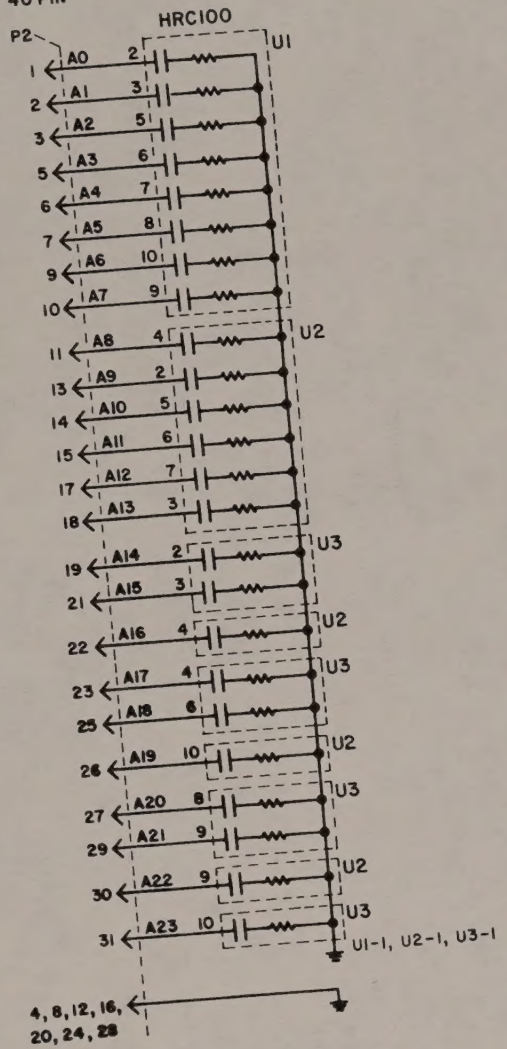
PART NUMBER	DESCRIPTION	QUANTITY PER
455460026	CONN PC EDG/SOLDTAIL26	1
455460040	CONN PC EDG/SOLDTAIL40	1
560440007	SCREW PHILIPS 4-40X7/16	4
575400007	WASHER FIBER .200 OD #4	4
575410002	WASHER FLAT SS .250 OD #4	4
706810021	PANEL (TERM PLUG) 6810	1
716810005	PC BD PREASS'Y 6810-5	1
HRC100	HYBRID TERMINATOR HRC100	5

End of report. 8 Details encountered.

26 PIN



40 PIN



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LeCroy RESEARCH SYSTEMS

6810-5

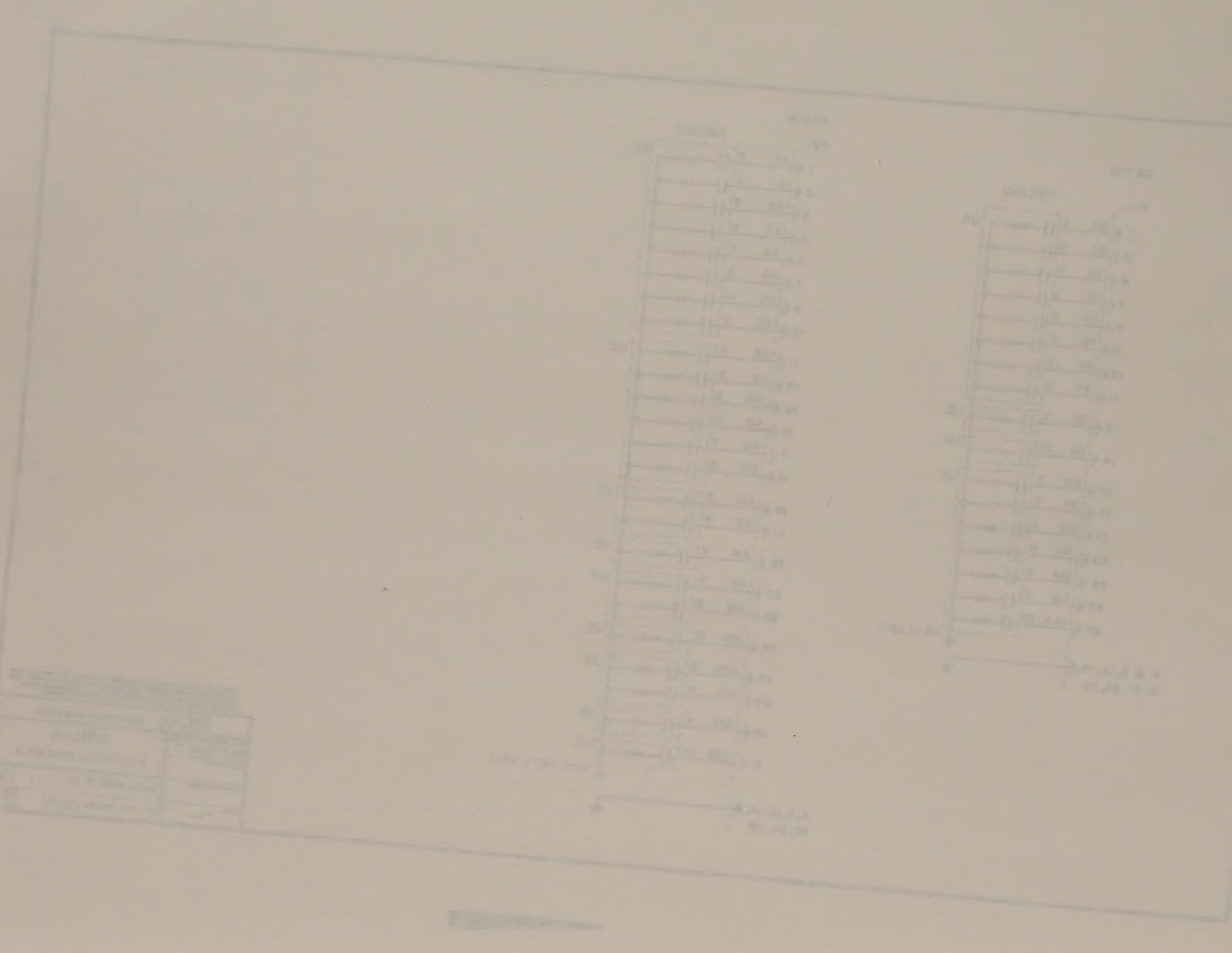
ELECTRICAL SCHEMATIC

DWG NO. 6810-5-SI

SIZE B

SH 1 OF 1

SOFTWARE 1001



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